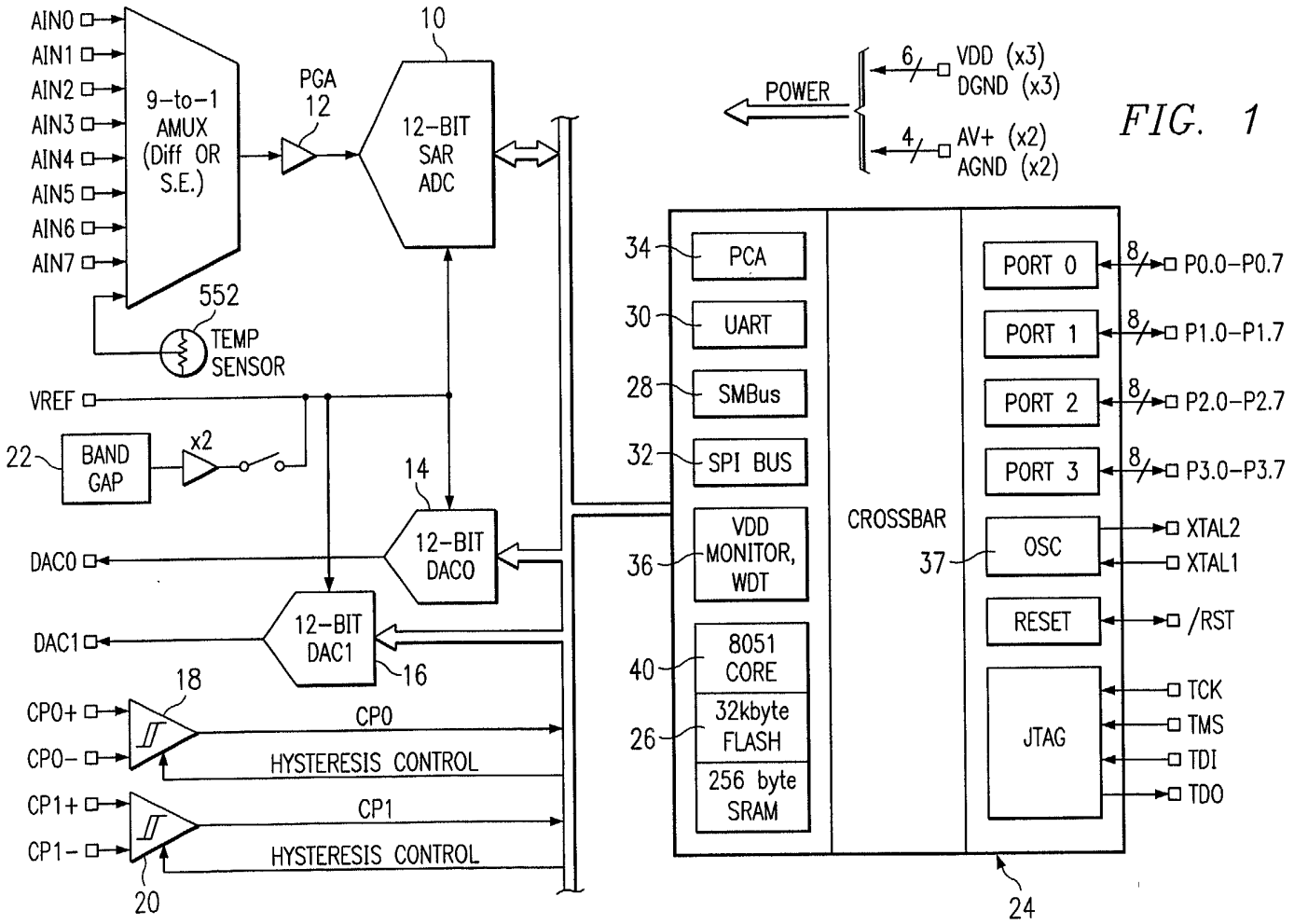

AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
9-to-1 AMUX (Diff OR S.E.)
PGA
12
10
12-BIT SAR ADC
552
TEMP SENSOR
VREF
22
BAND GAP
x2
14
12-BIT DAC0
DAC0
12-BIT DAC1
16
DAC1
18
CP0+
CP0-
CP0
HYSTERESIS CONTROL
CP1+
CP1-
CP1
HYSTERESIS CONTROL
20
POWER
6
VDD (x3)
DGND (x3)
4
AV+ (x2)
AGND (x2)
34
PCA
30
UART
28
SMBus
32
SPI BUS
36
VDD MONITOR, WDT
40
8051 CORE
26
32kbyte FLASH
256 byte SRAM
CROSSBAR
37
PORT 0
PORT 1
PORT 2
PORT 3
8
P0.0-P0.7
P1.0-P1.7
P2.0-P2.7
P3.0-P3.7
OSC
XTAL2
XTAL1
RESET
/RST
JTAG
TCK
TMS
TDI
TDO
24

FIG. 1

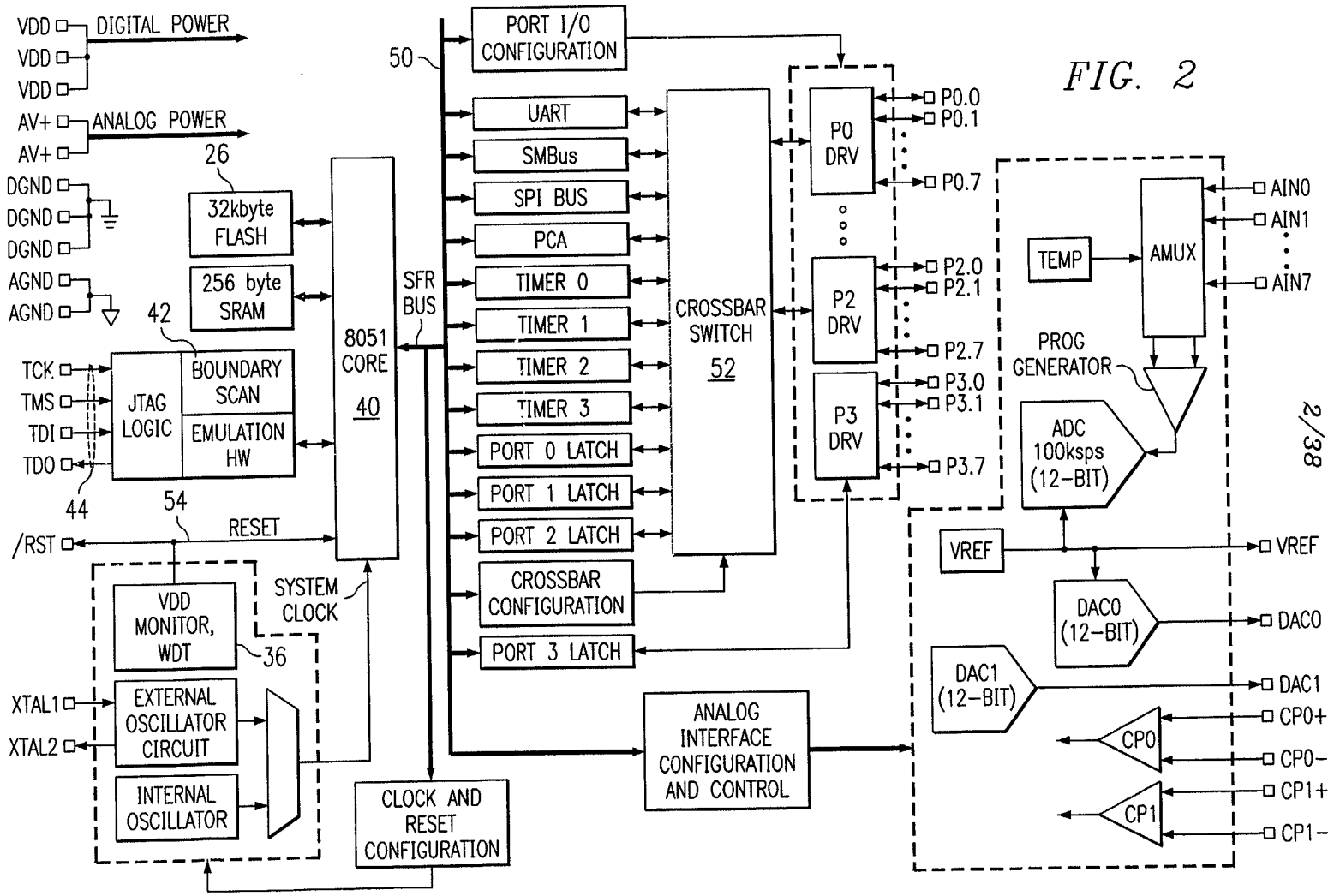

VDD
VDD
VDD
DIGITAL POWER
AV+
AV+
ANALOG POWER
DGND
DGND
DGND
AGND
AGND
26
32kbyte FLASH
256 byte SRAM
42
TCK
TMS
TDI
TDO
JTAG LOGIC
BOUNDARY SCAN
EMULATION HW
44
54
/RST
RESET
8051 CORE
40
SFR BUS
50
PORT I/O CONFIGURATION
UART
SMBus
SPI BUS
PCA
TIMER 0
TIMER 1
TIMER 2
TIMER 3
PORT 0 LATCH
PORT 1 LATCH
PORT 2 LATCH
CROSSBAR CONFIGURATION
PORT 3 LATCH
CROSSBAR SWITCH
52
P0 DRV
P2 DRV
P3 DRV
P0.0
P0.1
P0.7
P2.0
P2.1
P2.7
P3.0
P3.1
P3.7
TEMP
AMUX
AIN0
AIN1
AIN7
PROG GENERATOR
ADC 100ksps (12-BIT)
VREF
VREF
DAC0 (12-BIT)
DAC0
DAC1 (12-BIT)
DAC1
CP0+
CP0
CP0-
CP1+
CP1
CP1-
SYSTEM CLOCK
VDD MONITOR, WDT
36
XTAL1
XTAL2
EXTERNAL OSCILLATOR CIRCUIT
INTERNAL OSCILLATOR
CLOCK AND RESET CONFIGURATION
ANALOG INTERFACE CONFIGURATION AND CONTROL

FIG. 2

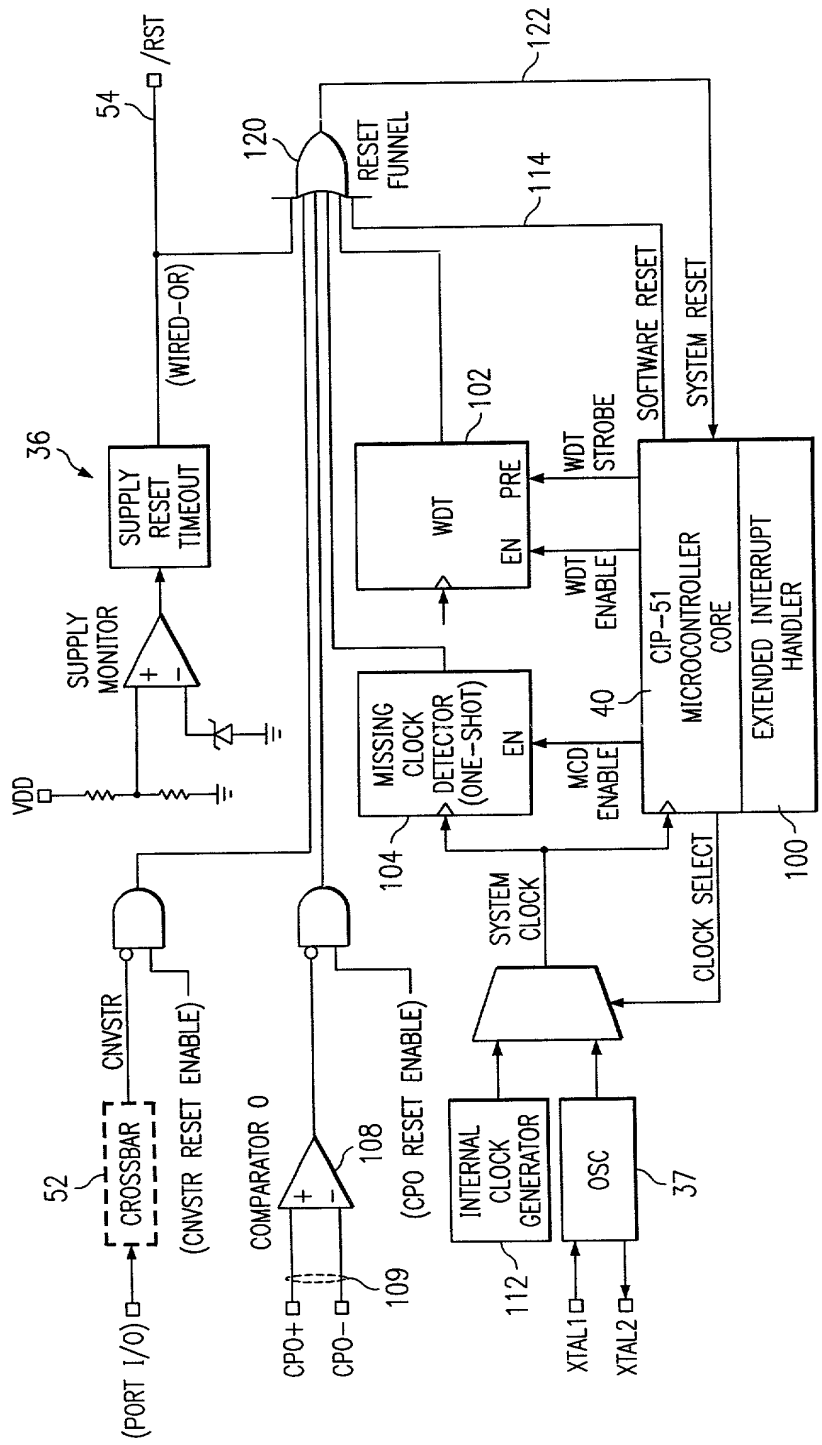

/RST
54
120
RESET FUNNEL
122
114
(WIRED-OR)
36
SUPPLY RESET TIMEOUT
SUPPLY MONITOR
VDD
WDT
102
PRE
EN
WDT STROBE
WDT ENABLE
SOFTWARE RESET
SYSTEM RESET
CIP-51 MICROCONTROLLER CORE
EXTENDED INTERRUPT HANDLER
MISSING CLOCK DETECTOR (ONE-SHOT)
EN
MCD ENABLE
40
104
100
CNVSTR
(CNVSTR RESET ENABLE)
52
CROSSBAR
(PORT I/O)
COMPARATOR 0
108
(CPO RESET ENABLE)
CPO+
CPO-
109
SYSTEM CLOCK
CLOCK SELECT
INTERNAL CLOCK GENERATOR
112
OSC
37
XTAL1
XTAL2

FIG. 3

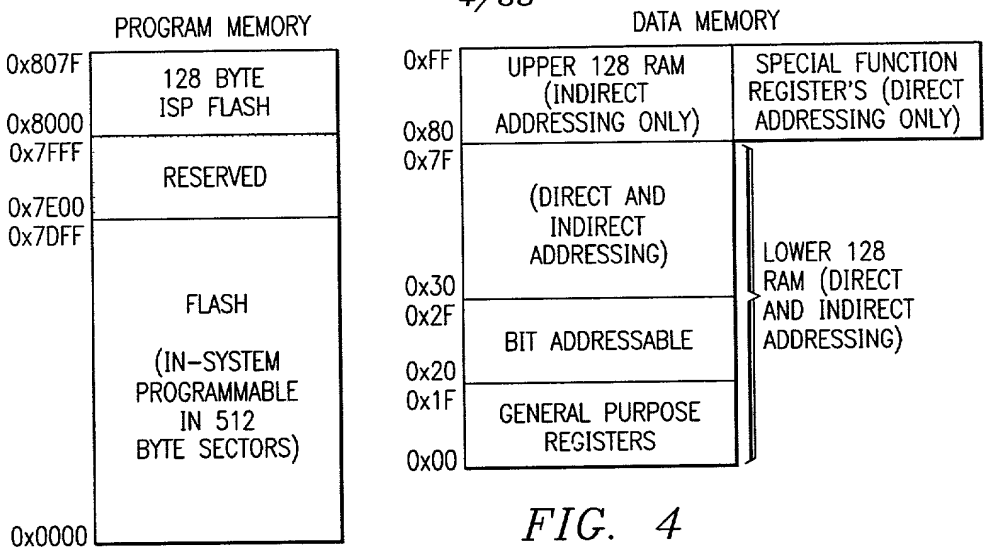

PROGRAM MEMORY
0x807F
128 BYTE ISP FLASH
0x8000
0x7FFF
RESERVED
0x7E00
0x7DFF
FLASH
(IN-SYSTEM PROGRAMMABLE IN 512 BYTE SECTORS)
0x0000
DATA MEMORY
0xFF
UPPER 128 RAM (INDIRECT ADDRESSING ONLY)
SPECIAL FUNCTION REGISTER'S (DIRECT ADDRESSING ONLY)
0x80
0x7F
(DIRECT AND INDIRECT ADDRESSING)
0x30
0x2F
BIT ADDRESSABLE
0x20
0x1F
GENERAL PURPOSE REGISTERS
0x00
LOWER 128 RAM (DIRECT AND INDIRECT ADDRESSING)

FIG. 4

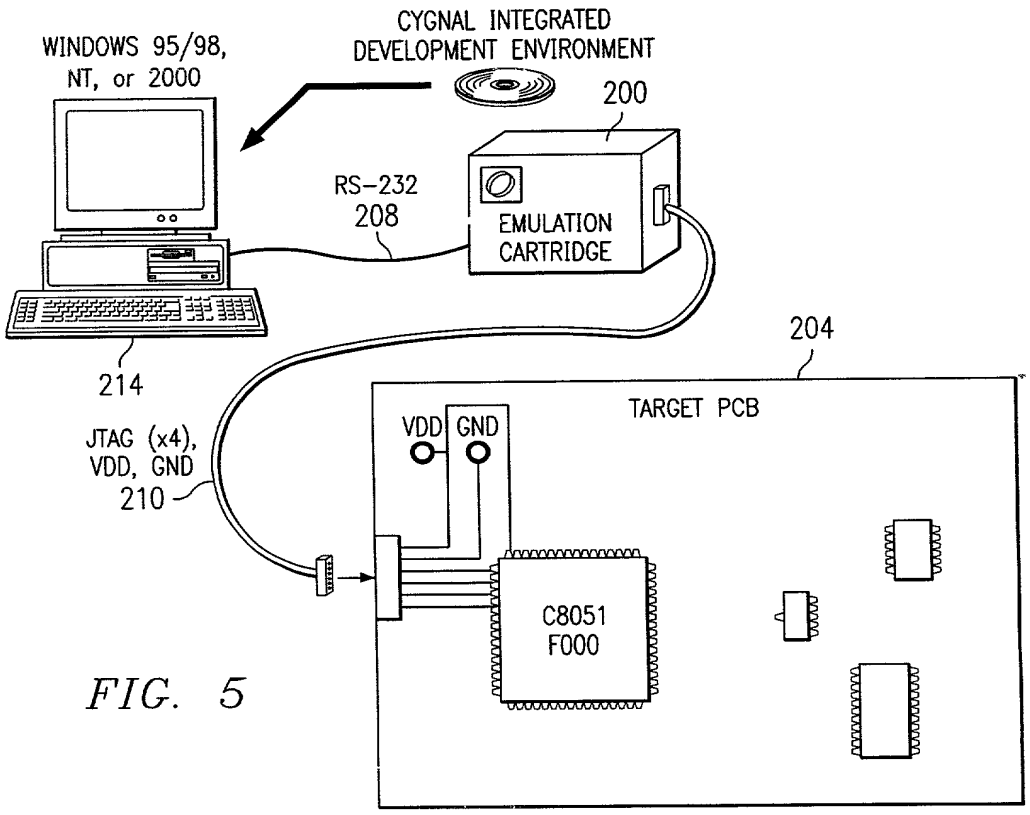

WINDOWS 95/98, NT, or 2000
CYGNAL INTEGRATED DEVELOPMENT ENVIRONMENT
200
RS-232
208
EMULATION CARTRIDGE
214
204
TARGET PCB
VDD
GND
JTAG (x4), VDD, GND
210
C8051
F000

FIG. 5

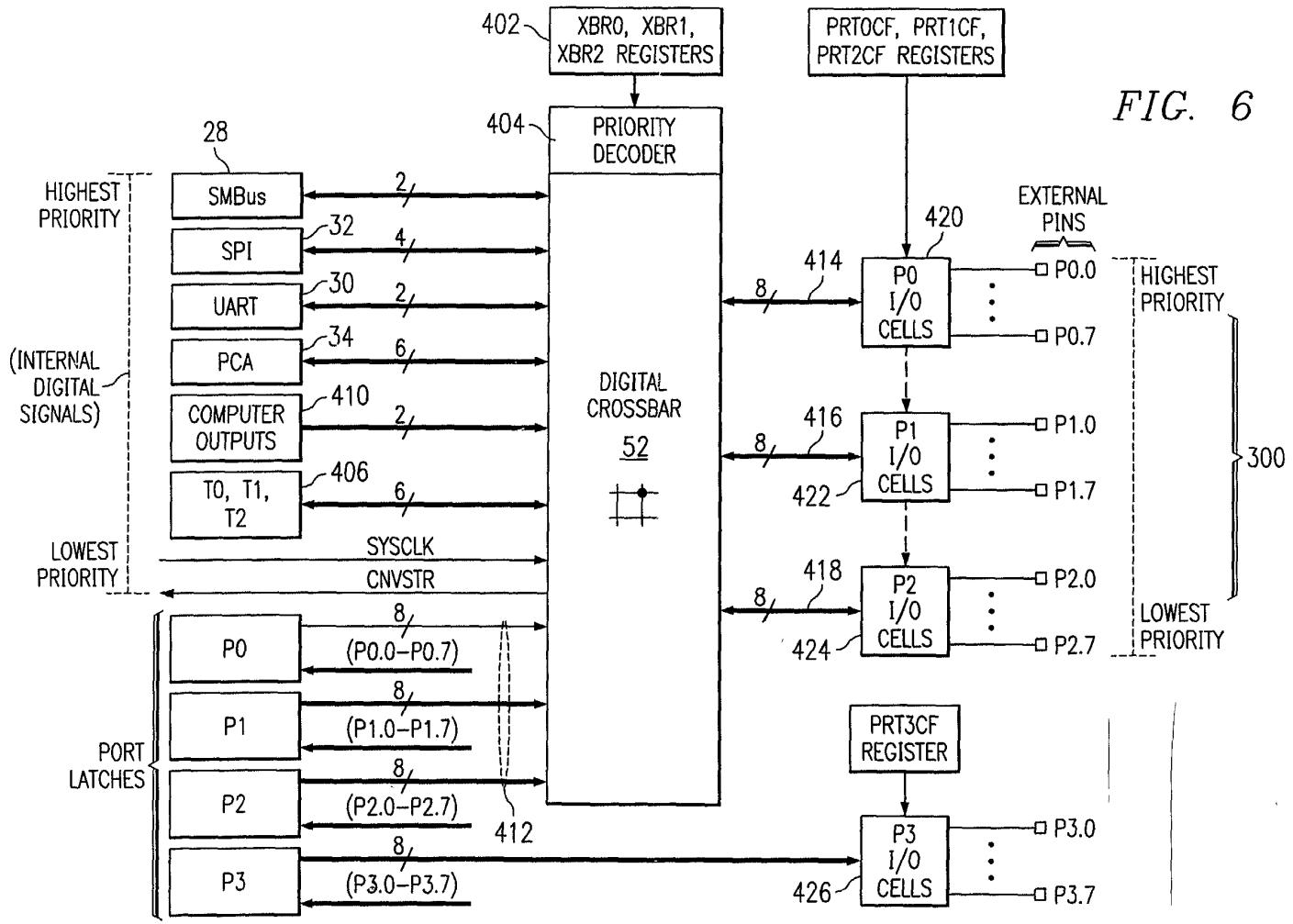

402
XBR0, XBR1, XBR2 REGISTERS
PRT0CF, PRT1CF, PRT2CF REGISTERS
404
PRIORITY DECODER
28
HIGHEST PRIORITY
SMBus
SPI
UART
PCA
COMPUTER OUTPUTS
T0, T1, T2
(INTERNAL DIGITAL SIGNALS)
LOWEST PRIORITY
2
32
4
30
2
34
6
410
2
406
6
SYSCLK
CNVSTR
DIGITAL CROSSBAR
52
8
(P0.0–P0.7)
(P1.0–P1.7)
(P2.0–P2.7)
(P3.0–P3.7)
PORT LATCHES
P0
P1
P2
P3
412
420
EXTERNAL PINS
414
P0 I/O CELLS
P0.0
P0.7
416
P1 I/O CELLS
422
P1.0
P1.7
418
P2 I/O CELLS
424
P2.0
P2.7
HIGHEST PRIORITY
LOWEST PRIORITY
300
PRT3CF REGISTER
P3 I/O CELLS
426
P3.0
P3.7

FIG. 6

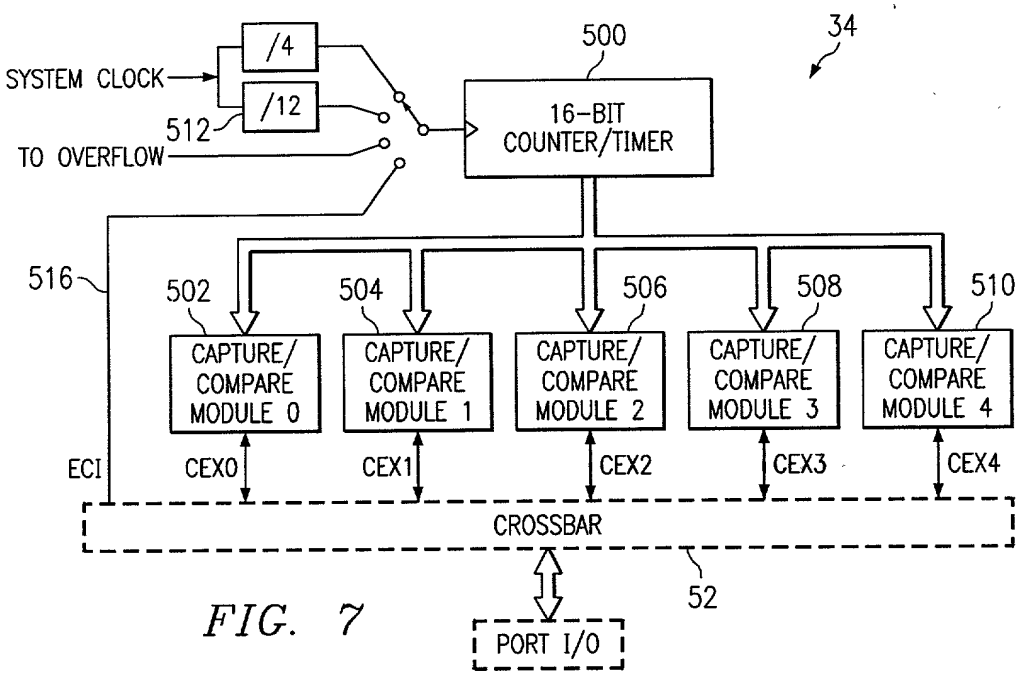

34
500
SYSTEM CLOCK
/4
/12
512
TO OVERFLOW
16-BIT COUNTER/TIMER
516
502
504
506
508
510
CAPTURE/ COMPARE MODULE 0
CAPTURE/ COMPARE MODULE 1
CAPTURE/ COMPARE MODULE 2
CAPTURE/ COMPARE MODULE 3
CAPTURE/ COMPARE MODULE 4
ECI
CEX0
CEX1
CEX2
CEX3
CEX4
CROSSBAR
52
PORT I/O

FIG. 7

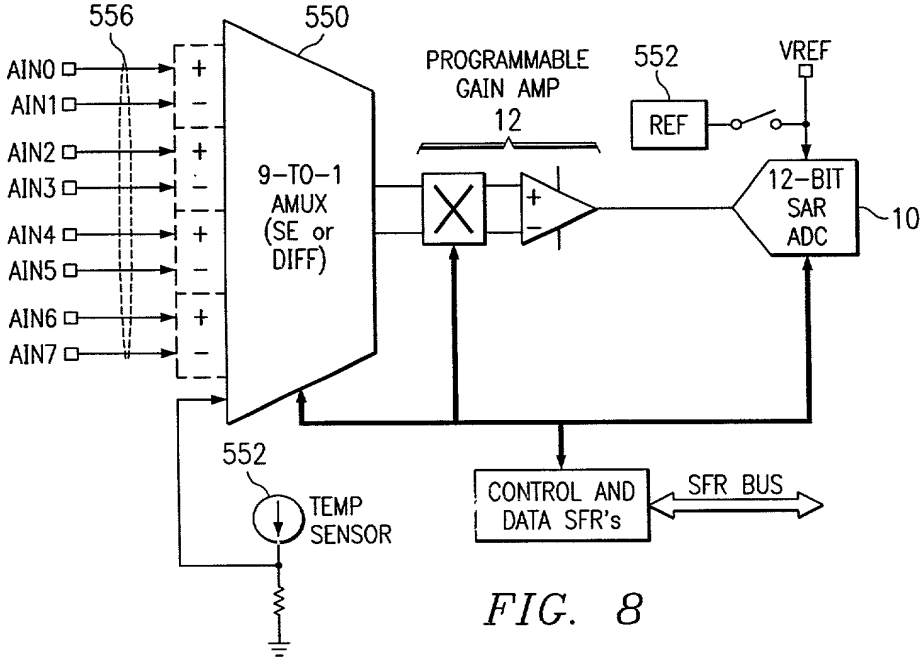

556
550
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
9-TO-1 AMUX (SE or DIFF)
PROGRAMMABLE GAIN AMP
12
552
REF
VREF
12-BIT SAR ADC
10
552
TEMP SENSOR
CONTROL AND DATA SFR's
SFR BUS

FIG. 8

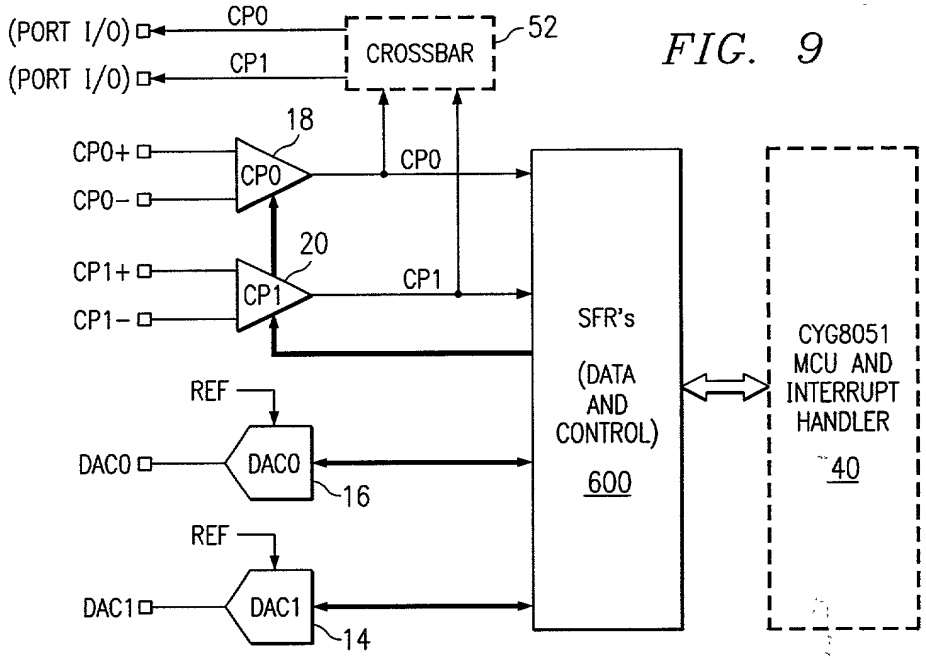
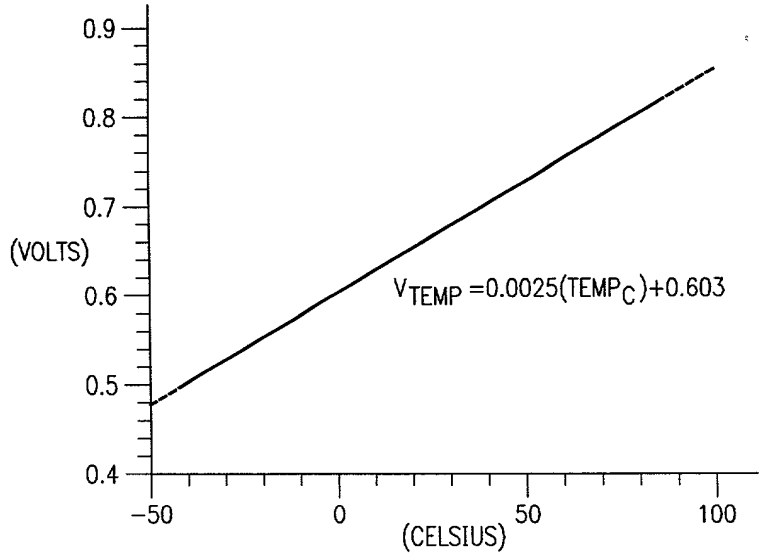

(PORT I/O)
(PORT I/O)
CP0
CP1
CROSSBAR
52
18
CP0+
CP0-
CP0
CP0
20
CP1+
CP1-
CP1
CP1
SFR's
(DATA
AND
CONTROL)
600
CYG8051
MCU AND
INTERRUPT
HANDLER
40
REF
DAC0
DAC0
16
REF
DAC1
DAC1
14

FIG. 9

FIG. 12


0.9
0.8
0.7
(VOLTS)
0.6
0.5
0.4
V_{TEMP} =0.0025($TEMP_C$)+0.603
-50
0
50
100
(CELSIUS)

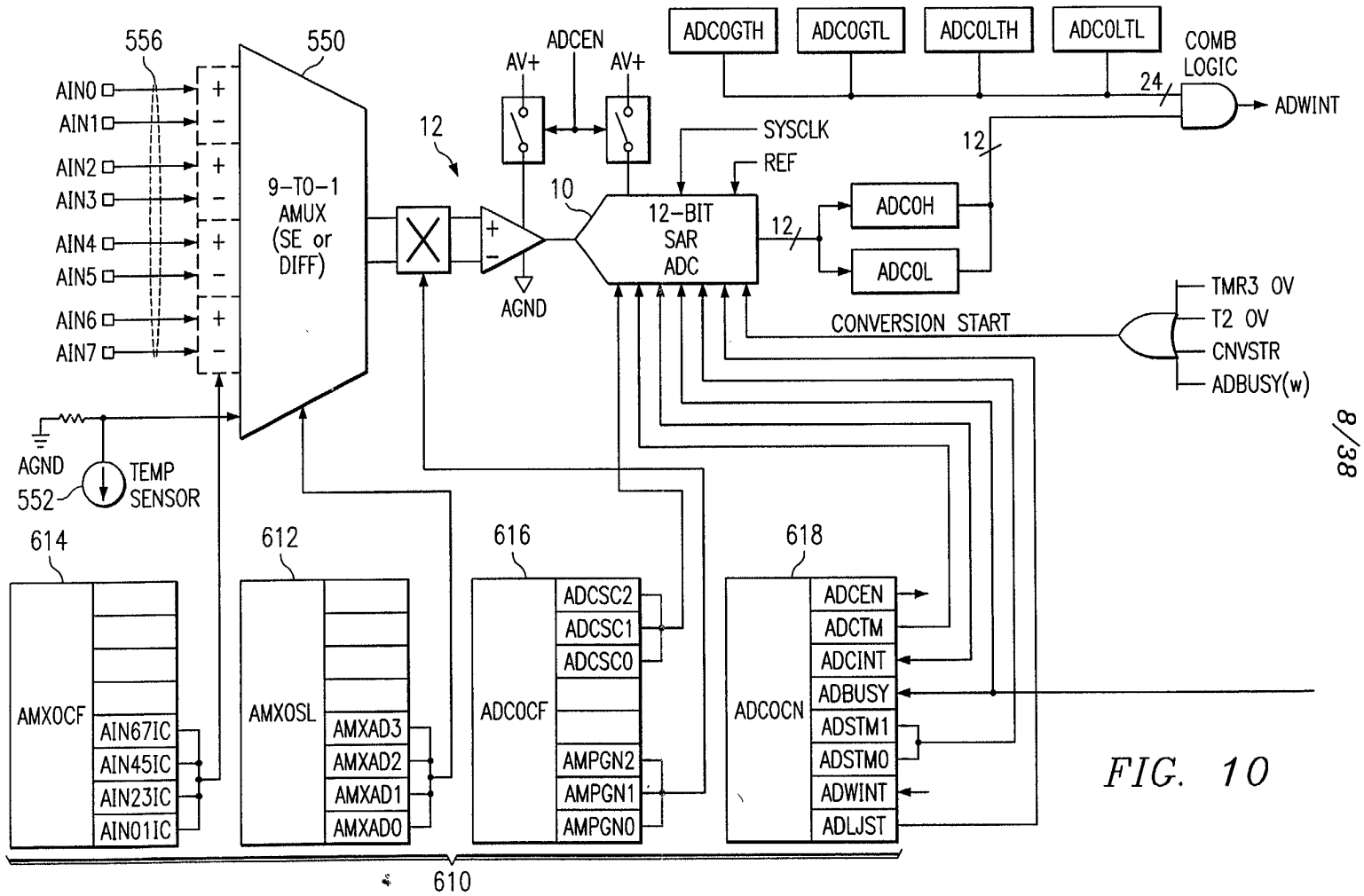

556
550
AIN0
AIN1
AIN2
AIN3
AIN4
AIN5
AIN6
AIN7
9-TO-1
AMUX
(SE or
DIFF)
12
ADCEN
AV+
AV+
ADC0GTH
ADC0GTL
ADC0LTH
ADC0LTL
COMB
LOGIC
24
ADWINT
SYSCLK
REF
10
12-BIT
SAR
ADC
12
12
ADC0H
ADC0L
AGND
CONVERSION START
TMR3 OV
T2 OV
CNVSTR
ADBUSY(w)
AGND
552
TEMP
SENSOR
614
612
616
618
AMX0CF
AIN67IC
AIN45IC
AIN23IC
AIN01IC
AMX0SL
AMXAD3
AMXAD2
AMXAD1
AMXAD0
ADC0CF
ADCSC2
ADCSC1
ADCSC0
AMPGN2
AMPGN1
AMPGN0
ADC0CN
ADCEN
ADCTM
ADCINT
ADBUSY
ADSTM1
ADSTM0
ADWINT
ADLJST
610

FIG. 10

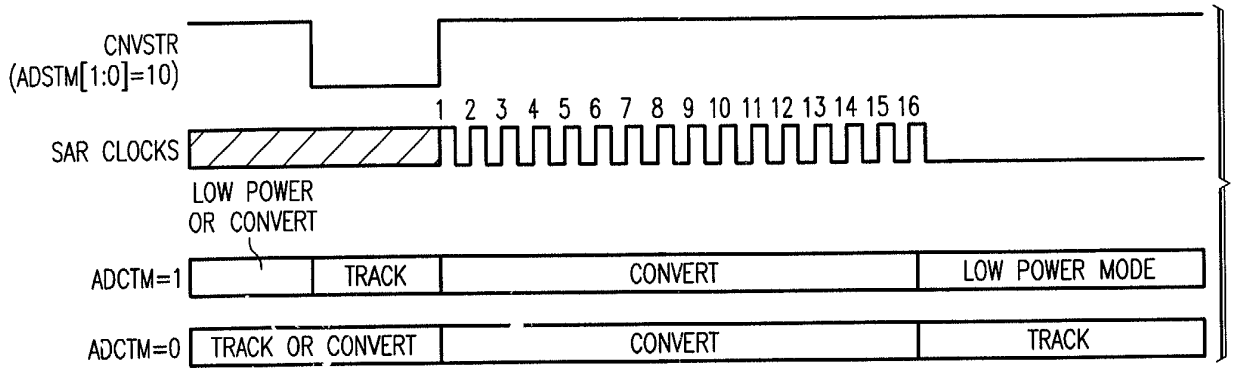


FIG. 11A

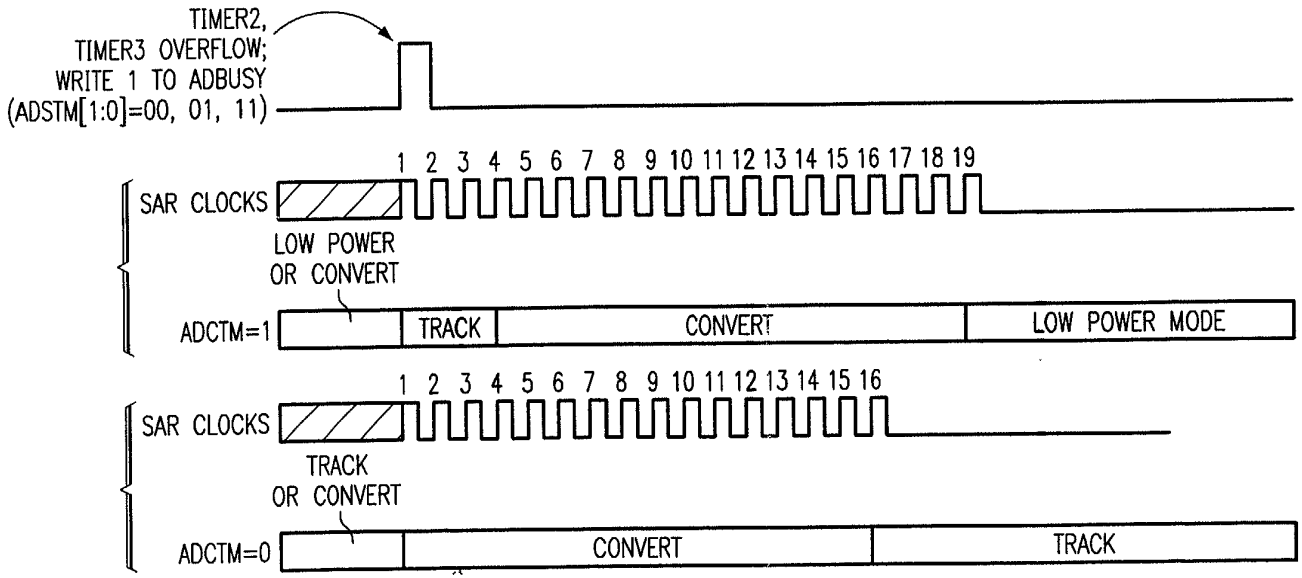


FIG. 11B

INPUT VOLTAGE (AD0–AGND)	ADC DATA WORD	
REF x (4095/4096)	0x0FFF	ADWINT NOT AFFECTED
	0x0201	
REF x (512/4096)	0x0200	ADC0LTH:ADC0LTL
	0x01FF	ADWINT=1
	0x0101	
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL
	0x00FF	ADWINT NOT AFFECTED
0	0x0000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADLJST=0,
ADC0LTH:ADC0LTL=0x0200,
ADC0GTH:ADC0GTL=0x0100.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x0200 AND > 0x0100.

INPUT VOLTAGE (AD0–AGND)	ADC DATA WORD	
REF x (4095/4096)	0x0FFF	ADWINT=1
	0x0201	
REF x (512/4096)	0x0200	ADC0GTH:ADC0GTL
	0x01FF	ADWINT NOT AFFECTED
	0x0101	
REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	ADWINT=1
0	0x0000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADLJST=0,
ADC0LTH:ADC0LTL=0x0100,
ADC0GTH:ADC0GTL=0x0200.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x0100 OR > 0x0200.

TO FIG. 13B

FIG. 13A

FIG. 13B

FROM FIG. 13A

INPUT VOLTAGE (AD0–AD1)	ADC DATA WORD	
REF x (4095/4096)	0x07FF	ADWINT NOT AFFECTED
	0x0101	
REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	ADWINT=1
	0x0000	
REF x (−1/4096)	0xFFFF	ADC0GTH:ADC0GTL
	0xFFFE	ADWINT NOT AFFECTED
−REF	0xF800	

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADLJST=0,
ADC0LTH:ADC0LTL=0x0100,
ADC0GTH:ADC0GTL=0xFFFF.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x0100 AND > 0xFFFF. (TWO'S COMPLEMENT MATH.)

INPUT VOLTAGE (AD0–AD1)	ADC DATA WORD	
REF x (4095/4096)	0x07FF	ADWINT=1
	0x0101	
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL
	0x00FF	ADWINT NOT AFFECTED
	0x0000	
REF x (−1/4096)	0xFFFF	ADC0LTH:ADC0LTL
	0xFFFE	ADWINT=1
−REF	0xF800	

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADLJST=0,
ADC0LTH:ADC0LTH=0xFFFF,
ADC0GTH:ADC0GTL=0x0100.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0xFFFF OR > 0x0100. (TWO'S COMPLEMENT MATH.)

INPUT VOLTAGE (AD0–AGND)	ADC DATA WORD	
REF x (4095/4096)	0xFFF0	ADWINT NOT AFFECTED
	0x2010	
REF x (512/4096)	0x2000	ADC0LTH:ADC0LTL
	0x1FF0	ADWINT=1
	0x1010	
REF x (256/4096)	0x1000	ADC0GTH:ADC0GTL
	0x0FF0	ADWINT NOT AFFECTED
0	0x0000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADLJST=1,
ADC0LTH:ADC0LTL=0x2000,
ADC0GTH:ADC0GTL=0x1000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x2000 AND > 0x1000.

INPUT VOLTAGE (AD0–AGND)	ADC DATA WORD	
REF x (4095/4096)	0xFFF0	ADWINT=1
	0x2010	
REF x (512/4096)	0x2000	ADC0GTH:ADC0GTL
	0x1FF0	ADWINT NOT AFFECTED
	0x1010	
REF x (256/4096)	0x1000	ADC0LTH:ADC0LTL
	0x0FF0	ADWINT=1
0	0x0000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x00, ADLJST=1,
ADC0LTH:ADC0LTL=0x1000,
ADC0GTH:ADC0GTL=0x2000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x1000 OR > 0x2000.

TO FIG. 14B

FIG. 14A

FROM FIG. 14A

FIG. 14B

INPUT VOLTAGE (AD0–AD1)	ADC DATA WORD	
REF x (4095/4096)	0x7FF0	ADWINT NOT AFFECTED
	0x1010	
REF x (256/4096)	0x1000	ADC0LTH:ADC0LTL
	0x0FF0	ADWINT=1
	0x0000	
REF x (−1/4096)	0xFFF0	ADC0GTH:ADC0GTL
	0xFFE0	ADWINT NOT AFFECTED
−REF	0x8000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADLJST=1,
ADC0LTH:ADC0LTL=0x1000,
ADC0GTH:ADC0GTL=0xFFF0.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0x1000 AND > 0xFFF0. (TWO'S COMPLEMENT MATH.)

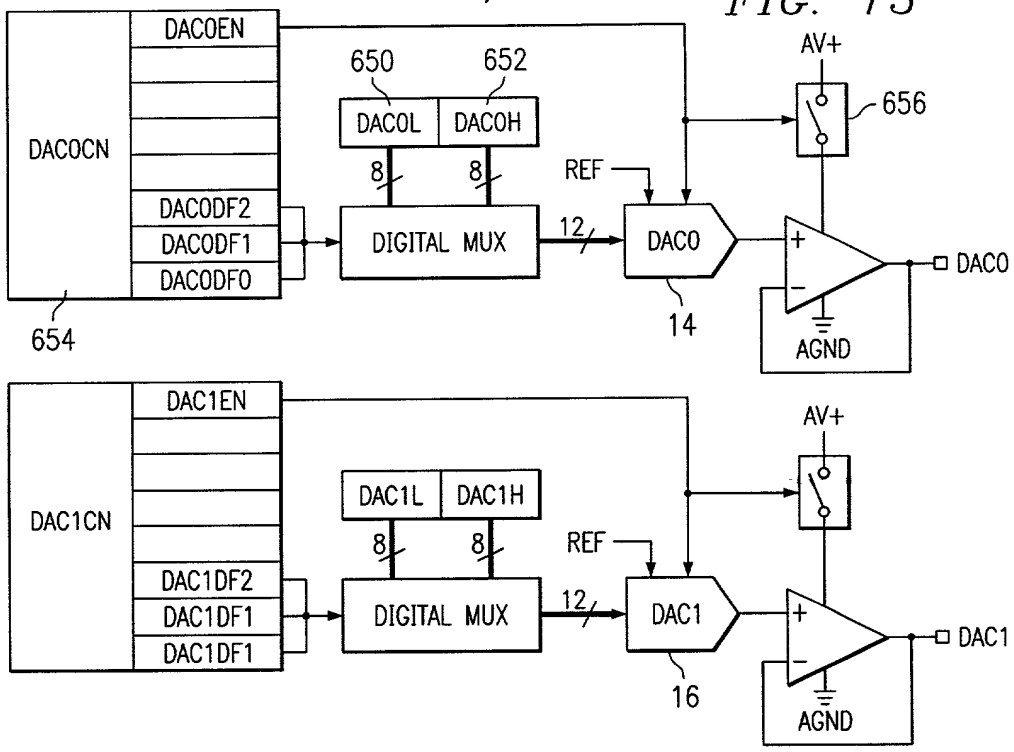
INPUT VOLTAGE (AD0–AD1)	ADC DATA WORD	
REF x (4095/4096)	0x7FF0	ADWINT=1
	0x1010	
REF x (256/4096)	0x1000	ADC0GTH:ADC0GTL
	0x0FF0	ADWINT NOT AFFECTED
	0x0000	
REF x (−1/4096)	0xFFF0	ADC0LTH:ADC0LTL
	0xFFE0	ADWINT=1
−REF	0x8000	

GIVEN:

AMX0SL=0x00, AMX0CF=0x01, ADLJST=1,
ADC0LTH:ADC0LTH=0xFFF0,
ADC0GTH:ADC0GTL=0x1000.

AN ADC END OF CONVERSION WILL CAUSE AN ADC WINDOW COMPARE INTERRUPT (ADWINT=1) IF THE RESULTING ADC DATA WORD IS < 0xFFF0 OR > 0x1000. (TWO'S COMPLEMENT MATH.)

FIG. 15


DAC0EN
DAC0CN
DAC0DF2
DAC0DF1
DAC0DF0
654
650
652
DAC0L
DAC0H
8
8
DIGITAL MUX
12
REF
DAC0
14
AV+
656
AGND
DAC0
DAC1EN
DAC1CN
DAC1DF2
DAC1DF1
DAC1DF1
DAC1L
DAC1H
8
8
DIGITAL MUX
12
REF
DAC1
16
AV+
AGND
DAC1

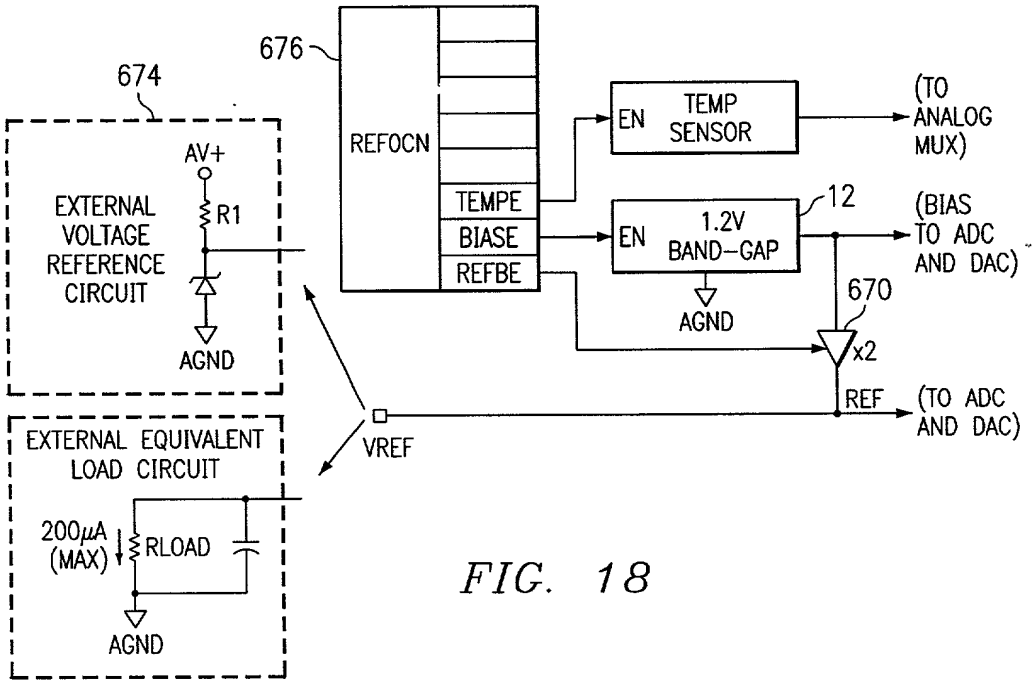

676
674
REFOCN
TEMPE
BIASE
REFBE
EN
TEMP SENSOR
(TO ANALOG MUX)
EN
1.2V BAND-GAP
12
(BIAS TO ADC AND DAC)
AGND
670
x2
REF
(TO ADC AND DAC)
EXTERNAL VOLTAGE REFERENCE CIRCUIT
AV+
R1
AGND
VREF
EXTERNAL EQUIVALENT LOAD CIRCUIT
200μA (MAX)
RLOAD
AGND

FIG. 18

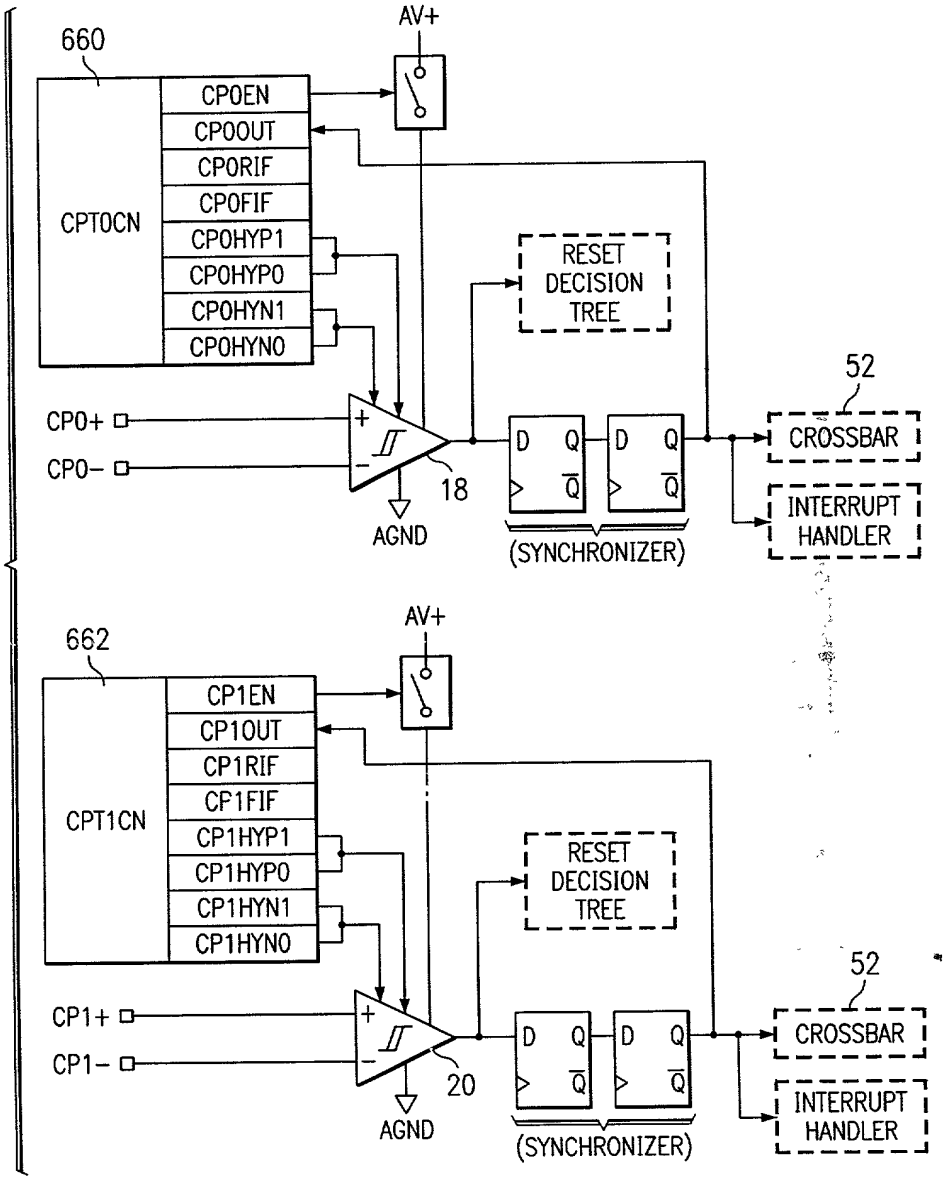

660
CPT0CN
CP0EN
CP0OUT
CP0RIF
CP0FIF
CP0HYP1
CP0HYP0
CP0HYN1
CP0HYN0
AV+
RESET DECISION TREE
52
CP0+
CP0−
18
AGND
D Q
Q
(SYNCHRONIZER)
CROSSBAR
INTERRUPT HANDLER
662
CPT1CN
CP1EN
CP1OUT
CP1RIF
CP1FIF
CP1HYP1
CP1HYP0
CP1HYN1
CP1HYN0
AV+
RESET DECISION TREE
52
CP1+
CP1−
20
AGND
D Q
Q
(SYNCHRONIZER)
CROSSBAR
INTERRUPT HANDLER

FIG. 16

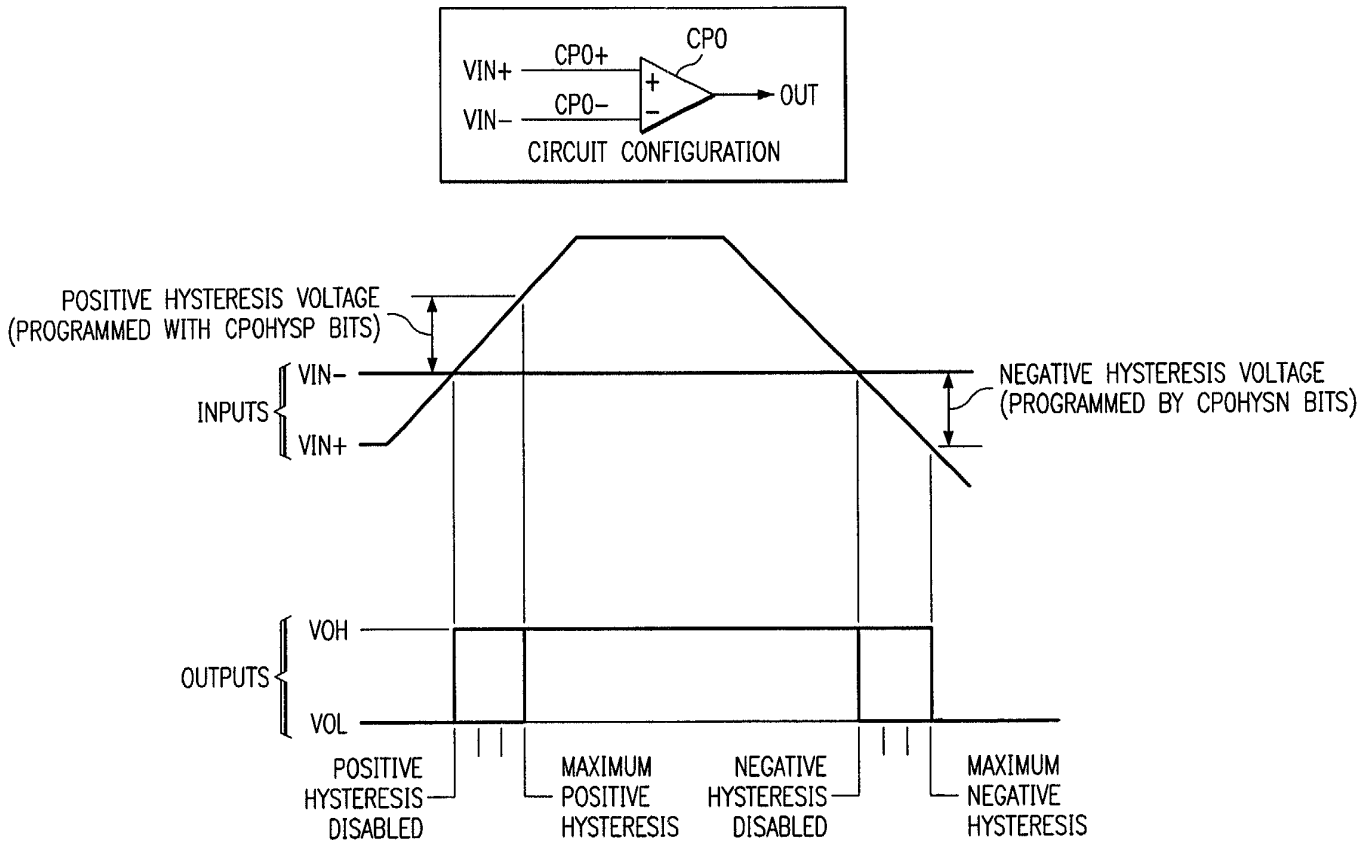
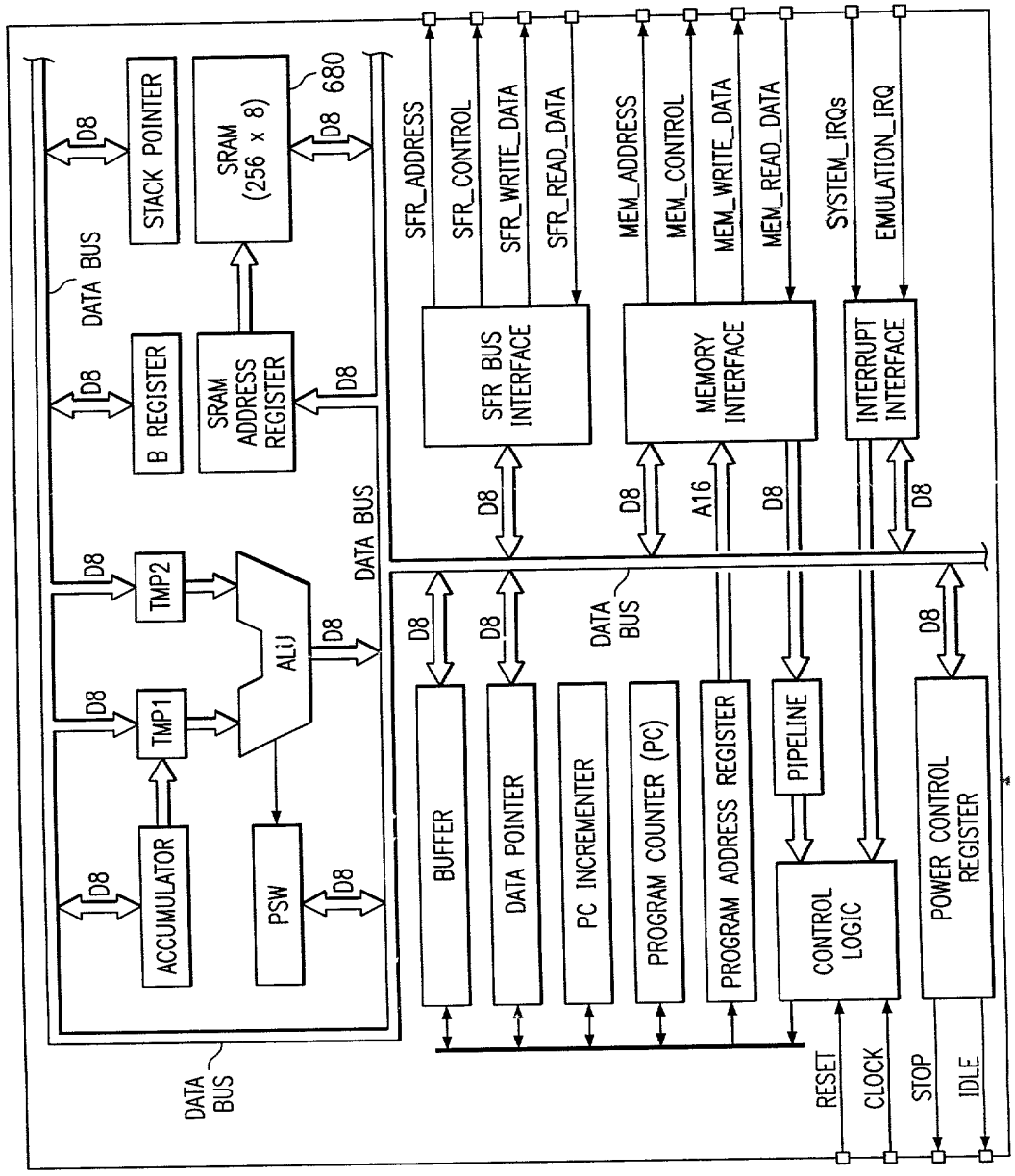

CPO
VIN+
CPO+
+
OUT
VIN−
CPO−
−
CIRCUIT CONFIGURATION
POSITIVE HYSTERESIS VOLTAGE
(PROGRAMMED WITH CPOHYSP BITS)
INPUTS
VIN−
VIN+
NEGATIVE HYSTERESIS VOLTAGE
(PROGRAMMED BY CPOHYSN BITS)
OUTPUTS
VOH
VOL
POSITIVE HYSTERESIS DISABLED
MAXIMUM POSITIVE HYSTERESIS
NEGATIVE HYSTERESIS DISABLED
MAXIMUM NEGATIVE HYSTERESIS

FIG. 17

FIG. 19


SFR_ADDRESS
SFR_CONTROL
SFR_WRITE_DATA
SFR_READ_DATA
MEM_ADDRESS
MEM_CONTROL
MEM_WRITE_DATA
MEM_READ_DATA
SYSTEM_IRQs
EMULATION_IRQ
SFR BUS INTERFACE
MEMORY INTERFACE
INTERRUPT INTERFACE
D8
A16
DATA BUS
STACK POINTER
SRAM (256 x 8)
680
B REGISTER
SRAM ADDRESS REGISTER
TMP2
TMP1
ALU
ACCUMULATOR
PSW
BUFFER
DATA POINTER
PC INCREMENTER
PROGRAM COUNTER (PC)
PROGRAM ADDRESS REGISTER
PIPELINE
CONTROL LOGIC
POWER CONTROL REGISTER
RESET
CLOCK
STOP
IDLE

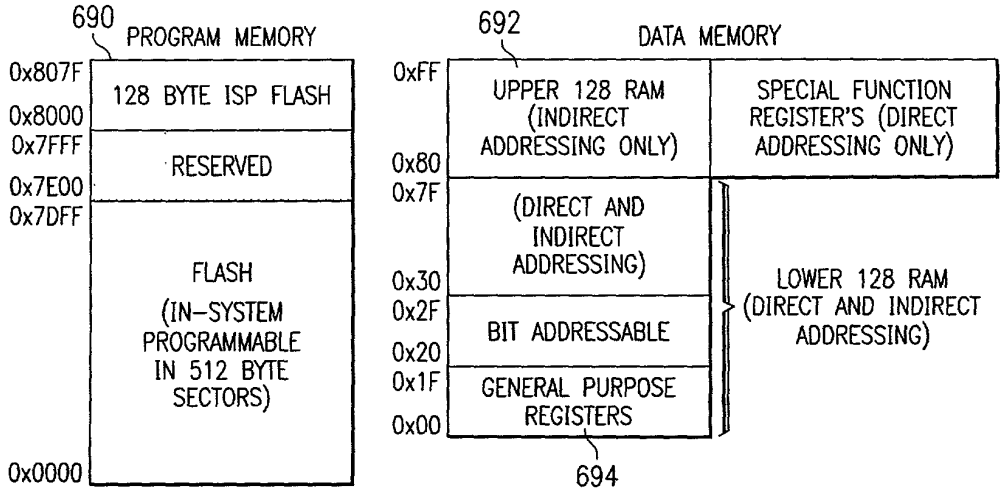

690
PROGRAM MEMORY
0x807F
0x8000
0x7FFF
0x7E00
0x7DFF
0x0000
128 BYTE ISP FLASH
RESERVED
FLASH
(IN–SYSTEM PROGRAMMABLE IN 512 BYTE SECTORS)
692
DATA MEMORY
0xFF
0x80
0x7F
0x30
0x2F
0x20
0x1F
0x00
UPPER 128 RAM (INDIRECT ADDRESSING ONLY)
SPECIAL FUNCTION REGISTER'S (DIRECT ADDRESSING ONLY)
(DIRECT AND INDIRECT ADDRESSING)
BIT ADDRESSABLE
GENERAL PURPOSE REGISTERS
LOWER 128 RAM (DIRECT AND INDIRECT ADDRESSING)
694

FIG. 20

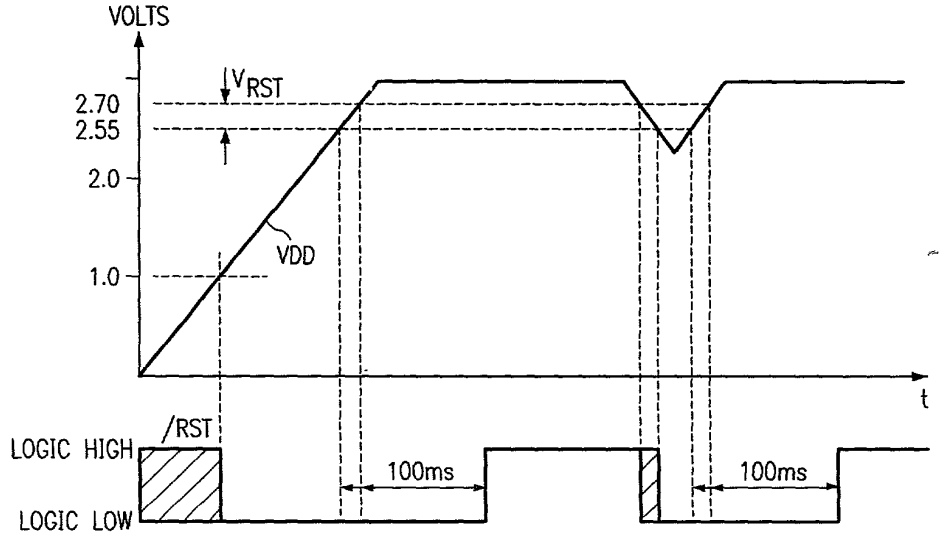
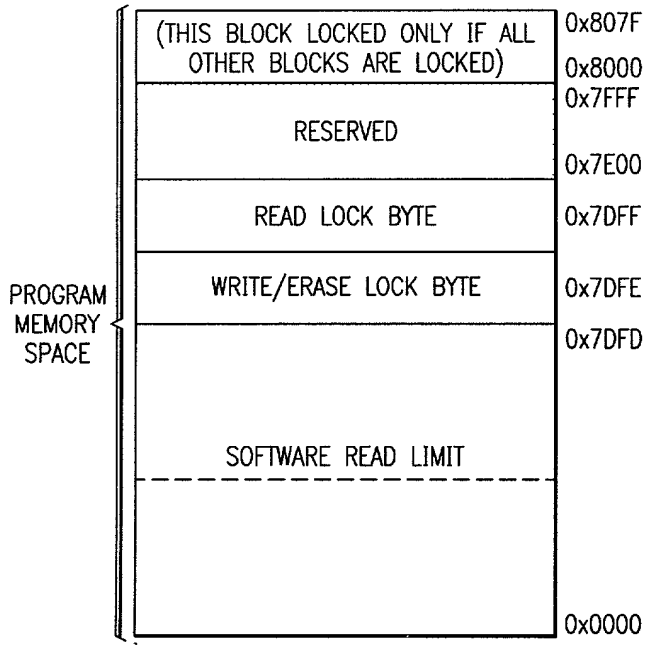

VOLTS
2.70
2.55
2.0
1.0
VRST
VDD
t
/RST
LOGIC HIGH
LOGIC LOW
100ms
100ms

FIG. 22



READ AND WRITE/ ERASE SECURITY BITS. (BIT 7 IS MSB.)

BIT	MEMORY BLOCK
7	0x7000–0x7DFD
6	0x6000–0x6FFF
5	0x5000–0x5FFF
4	0x4000–0x4FFF
3	0x3000–0x3FFF
2	0x2000–0x2FFF
1	0x1000–0x1FFF
0	0x0000–0x0FFF

FLASH READ LOCK BYTE

BITS7–0: EACH BIT LOCKS A CORRESPONDING BLOCK OF MEMORY. (BIT 7 IS MSB.)
0: READ OPERATIONS ARE LOCKED (DISABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.
1: READ OPERATIONS ARE UNLOCKED (ENABLED) FOR CORRESPONDING BLOCK ACCROSS THE JTAG INTERFACE.

FLASH WRITE/ERASE LOCK BYTE

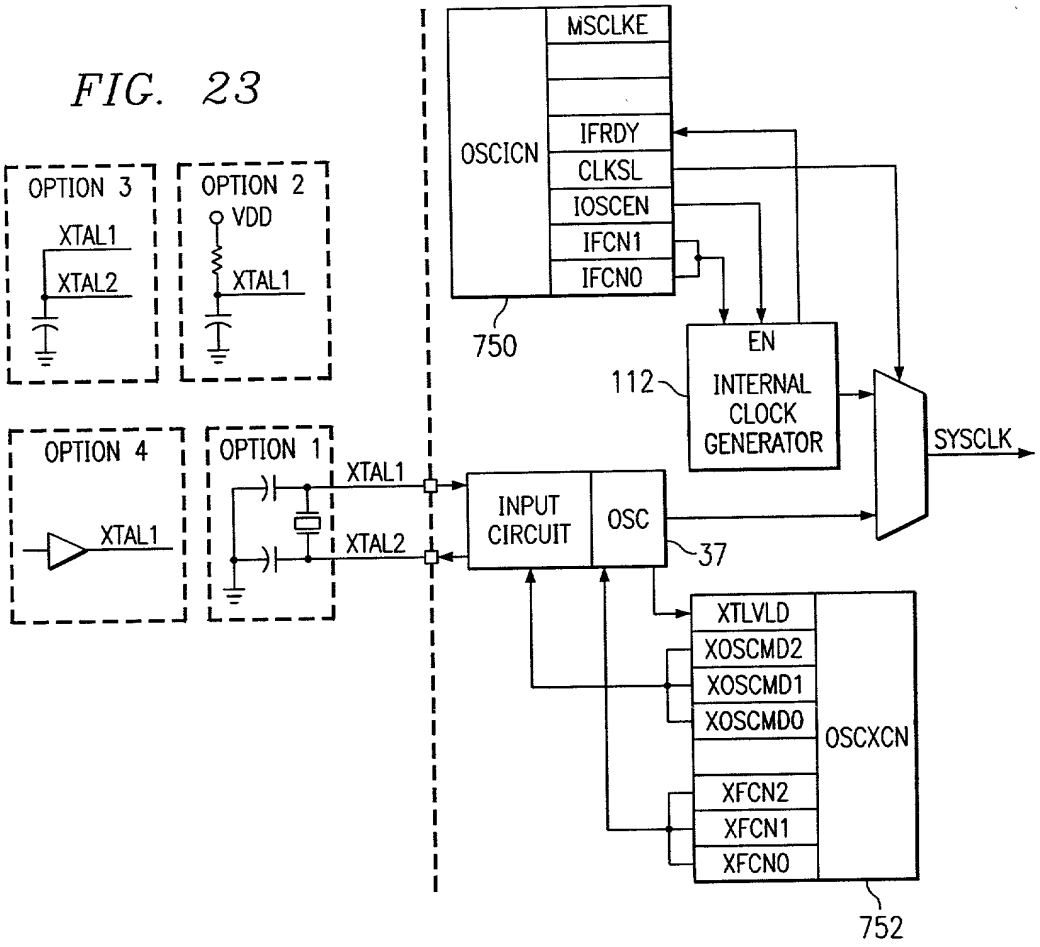
BITS 7–0: EACH BIT LOCKS A CORRESPONDING BLOCK OF MEMORY.
0: WRITE/ERASE OPERATIONS ARE LOCKED (DISABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.
1: WRITE/ERASE OPERATIONS ARE UNLOCKED (ENABLED) FOR CORRESPONDING BLOCK ACROSS THE JTAG INTERFACE.

FLASH ACCESS LIMIT REGISTER (FLACL)

THE CONTENT OF THIS REGISTER IS USED AS THE HIGH BYTE OF THE 16-BIT SOFTWARE READ LIMIT ADDRESS. THE 16-BIT READ LIMIT ADDRESS VALUE IS CALCULATED AS 0xNN00 WHERE NN IS REPLACED BY CONTENT OF THIS REGISTER ON RESET. SOFTWARE RUNNING AT OR ABOVE THIS ADDRESS IS PROHIBITED FROM USING THE MOVX AND MOVC INSTRUCTIONS TO READ, WRITE, OR ERASE, LOCATIONS BELOW THIS ADDRESS. ANY ATTEMPTS TO READ LOCATIONS BELOW THIS LIMIT WILL RETURN THE VALUE 0x00.

FIG. 21

FIG. 23


OPTION 3
XTAL1
XTAL2
OPTION 2
VDD
XTAL1
OPTION 4
XTAL1
OPTION 1
XTAL1
XTAL2
OSCICN
MSCLKE
IFRDY
CLKSL
IOSCEN
IFCN1
IFCN0
750
EN
112
INTERNAL CLOCK GENERATOR
SYSCLK
INPUT CIRCUIT
OSC
37
XTLVLD
XOSCMD2
XOSCMD1
XOSCMD0
XFCN2
XFCN1
XFCN0
OSCXCN
752

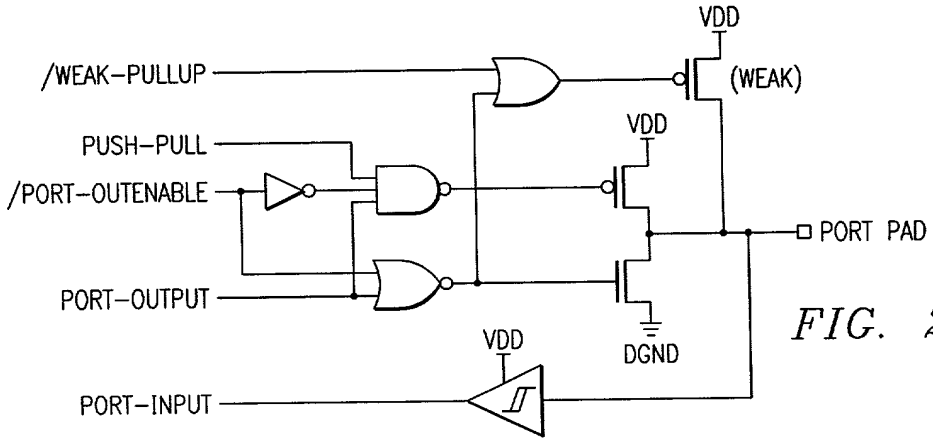
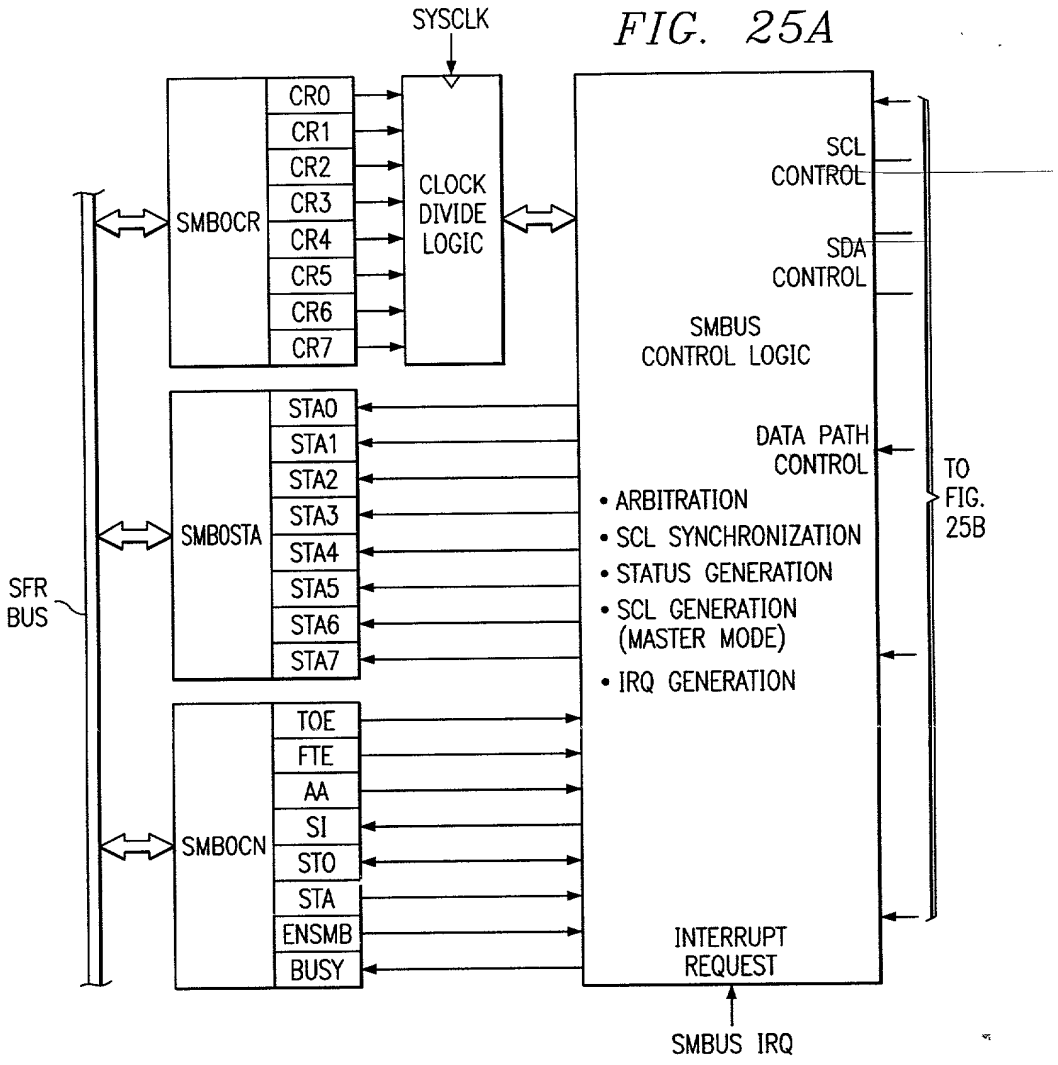

VDD
/WEAK-PULLUP
(WEAK)
VDD
PUSH-PULL
/PORT-OUTENABLE
PORT PAD
PORT-OUTPUT
DGND
VDD
PORT-INPUT

FIG. 24

FIG. 25A



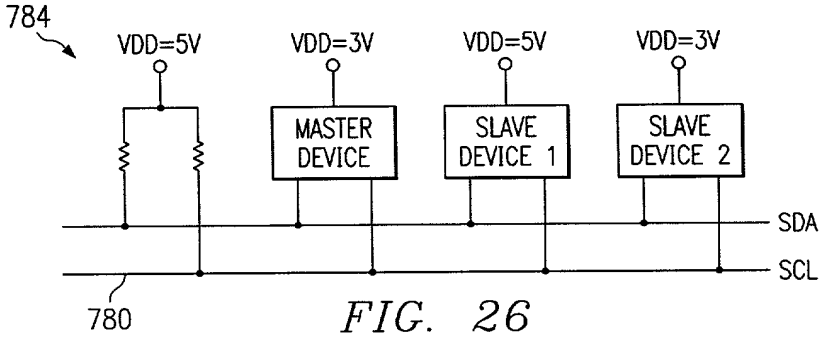


FIG. 26

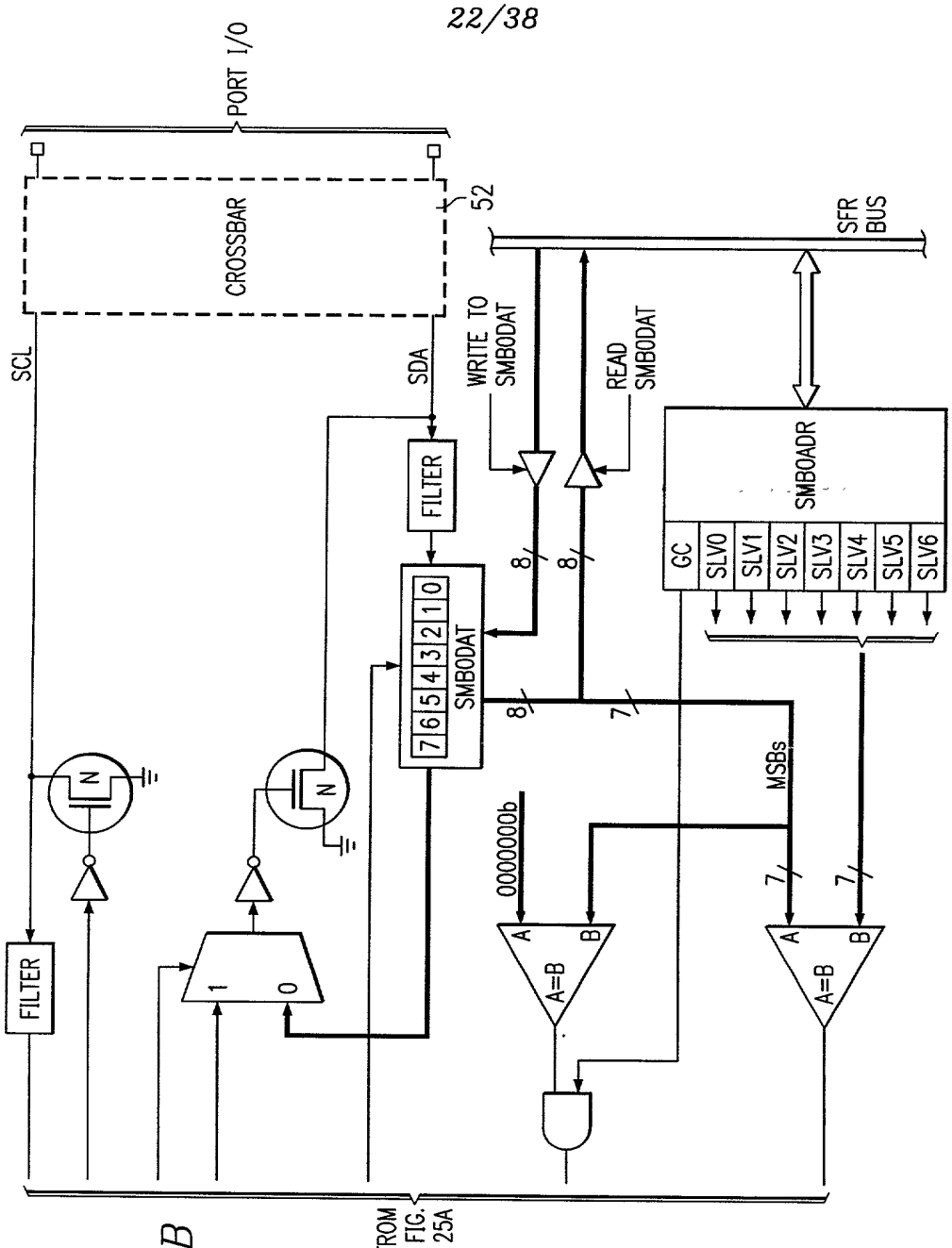
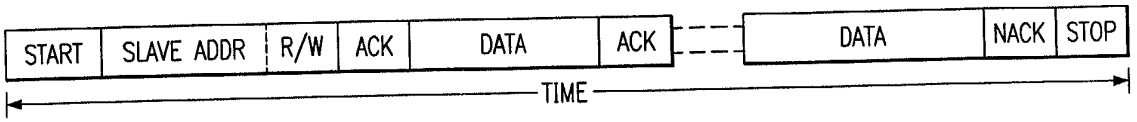

PORT I/O
CROSSBAR
52
SFR BUS
SCL
SDA
WRITE TO SMB0DAT
READ SMB0DAT
FILTER
SMB0ADR
GC
SLV0
SLV1
SLV2
SLV3
SLV4
SLV5
SLV6
8
7 6 5 4 3 2 1 0
SMB0DAT
MSBs
0000000b
A
B
A=B
FILTER
FROM FIG. 25A

FIG. 25B

FIG. 27


START
SLAVE ADDR
R/W
ACK
DATA
ACK
DATA
NACK
STOP
TIME

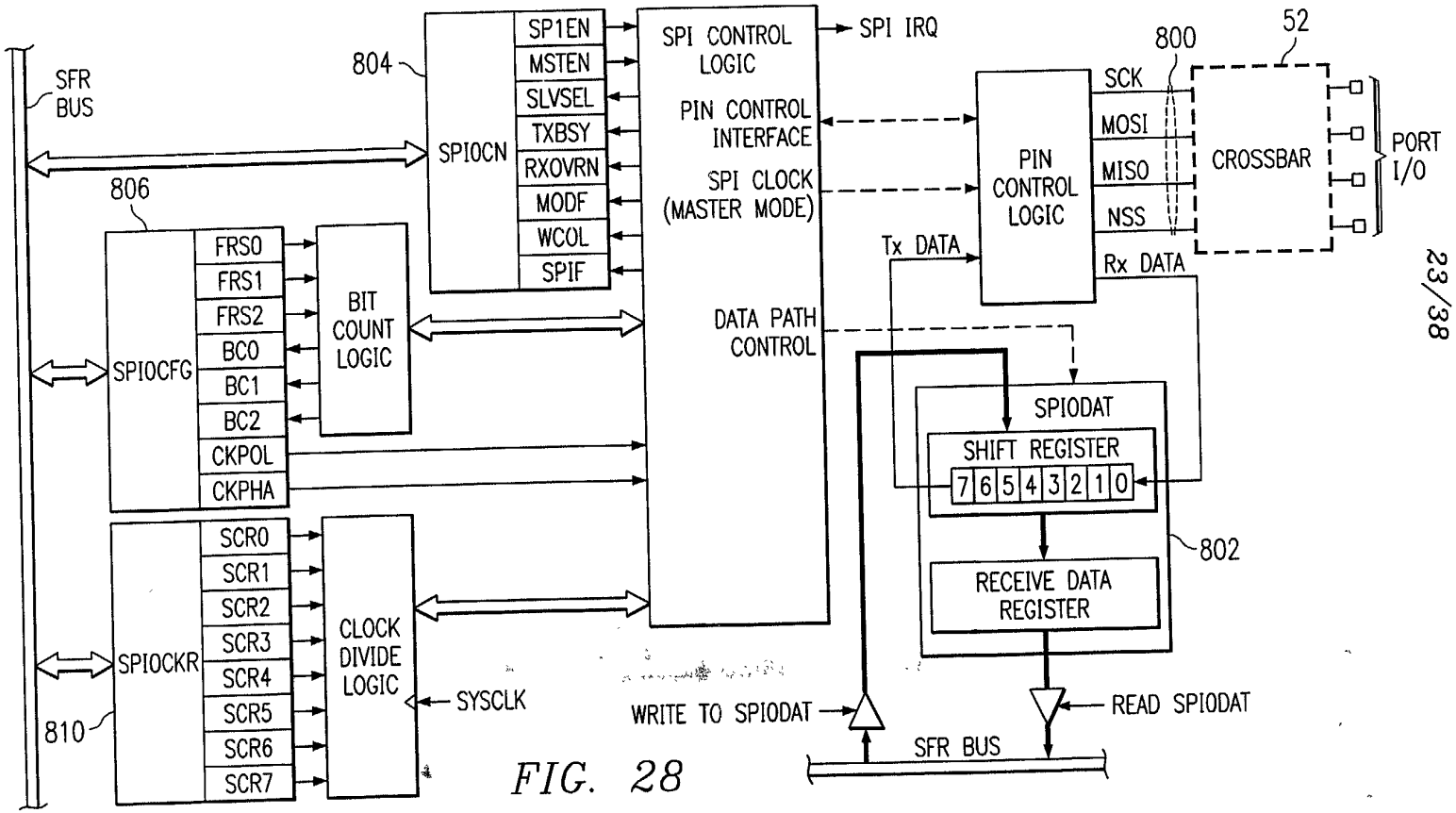

SFR BUS
804
SPI0CN
SP1EN
MSTEN
SLVSEL
TXBSY
RXOVRN
MODF
WCOL
SPIF
SPI CONTROL LOGIC
SPI IRQ
PIN CONTROL INTERFACE
SPI CLOCK (MASTER MODE)
DATA PATH CONTROL
800
52
SCK
MOSI
MISO
NSS
CROSSBAR
PORT I/O
PIN CONTROL LOGIC
Tx DATA
Rx DATA
806
SPI0CFG
FRS0
FRS1
FRS2
BC0
BC1
BC2
CKPOL
CKPHA
BIT COUNT LOGIC
SPI0DAT
SHIFT REGISTER
7 6 5 4 3 2 1 0
802
RECEIVE DATA REGISTER
SPI0CKR
SCR0
SCR1
SCR2
SCR3
SCR4
SCR5
SCR6
SCR7
CLOCK DIVIDE LOGIC
SYSCLK
810
WRITE TO SPI0DAT
READ SPI0DAT
SFR BUS

FIG. 28

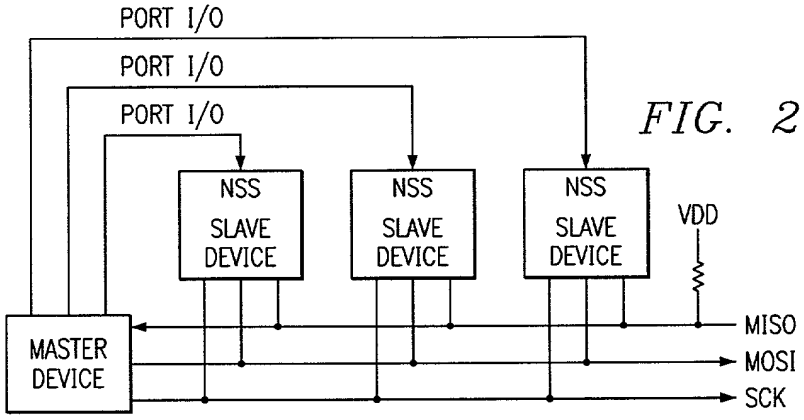


FIG. 29

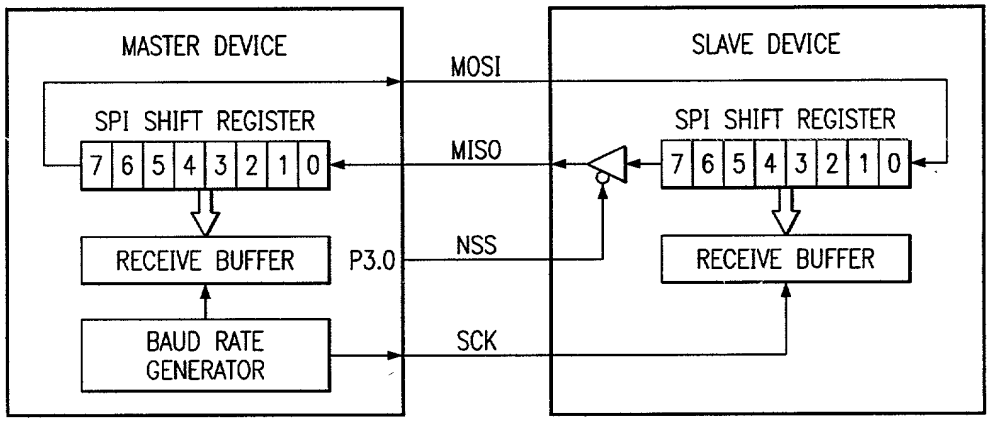


FIG. 30

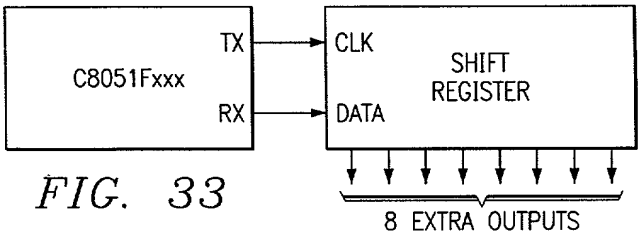


FIG. 33

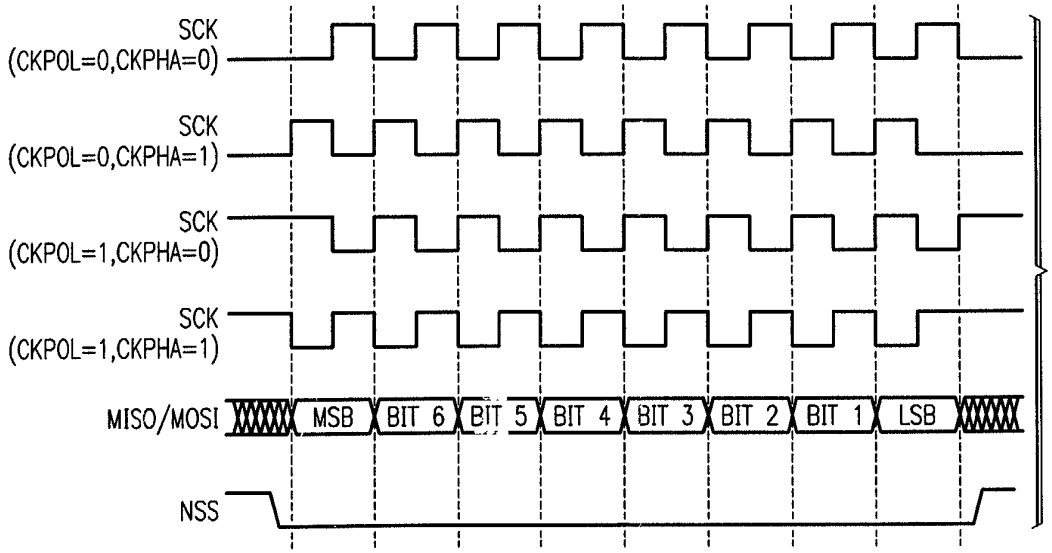

SCK
(CKPOL=0,CKPHA=0)
SCK
(CKPOL=0,CKPHA=1)
SCK
(CKPOL=1,CKPHA=0)
SCK
(CKPOL=1,CKPHA=1)
MISO/MOSI
MSB
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
LSB
NSS

FIG. 31

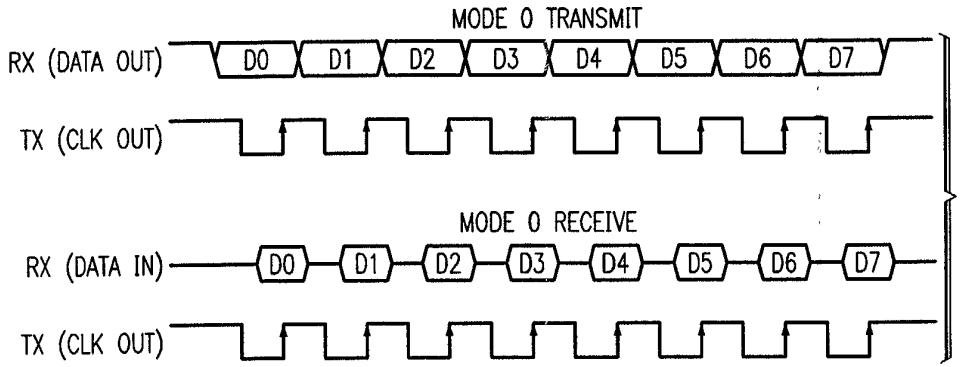

MODE 0 TRANSMIT
RX (DATA OUT)
D0
D1
D2
D3
D4
D5
D6
D7
TX (CLK OUT)
MODE 0 RECEIVE
RX (DATA IN)
D0
D1
D2
D3
D4
D5
D6
D7
TX (CLK OUT)

FIG. 34

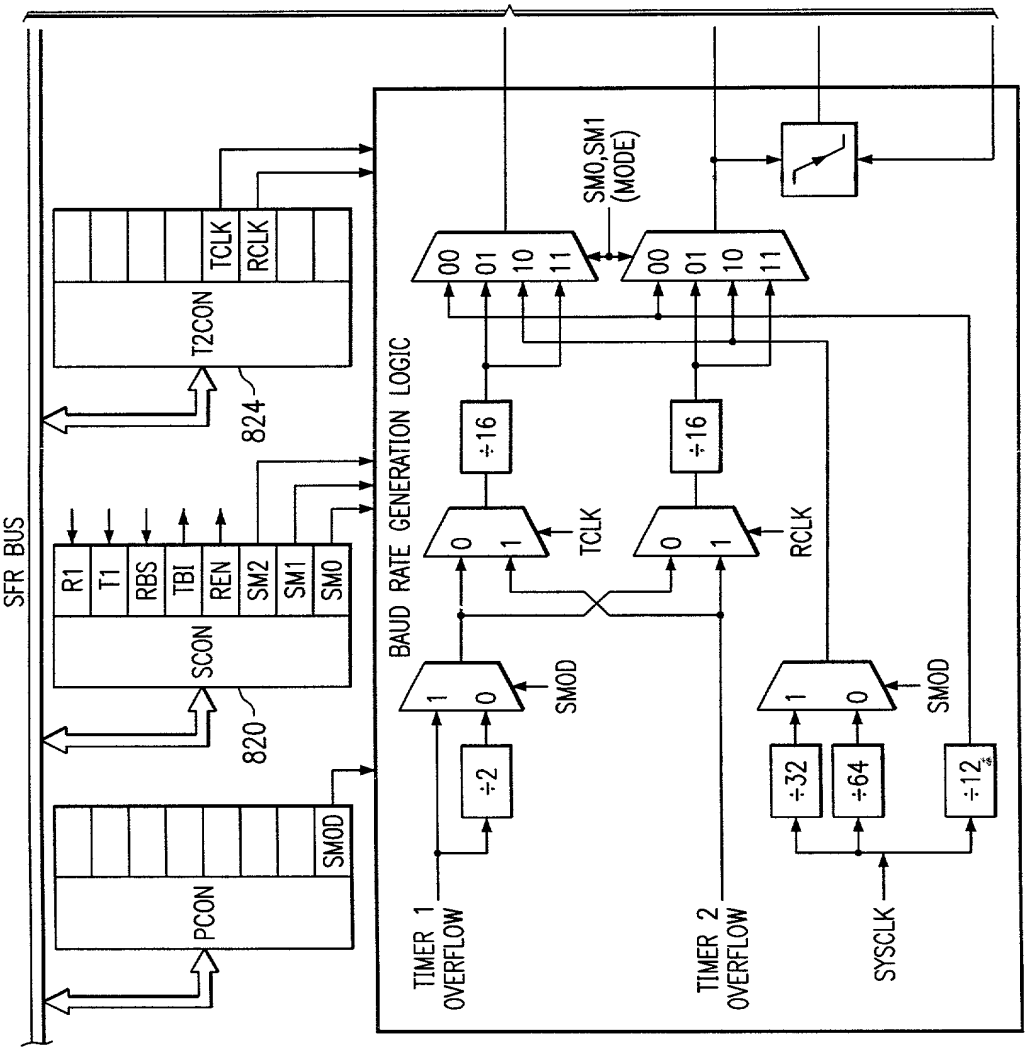
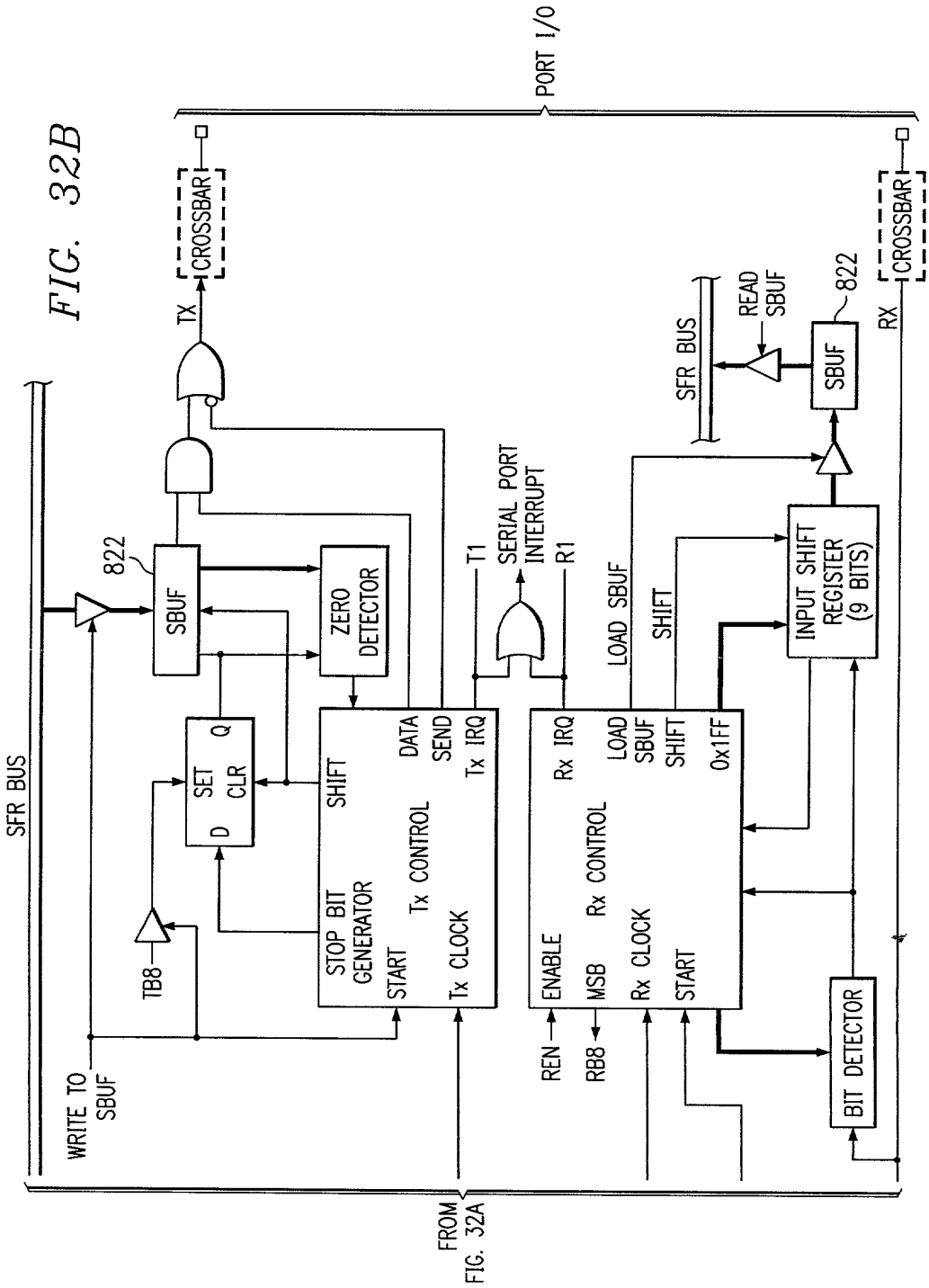

TO FIG. 32B
SFR BUS
T2CON
TCLK
RCLK
824
SCON
R1
T1
RBS
TBI
REN
SM2
SM1
SM0
820
PCON
SMOD
BAUD RATE GENERATION LOGIC
SM0,SM1
(MODE)
00
01
10
11
÷16
÷16
TCLK
RCLK
0
1
SMOD
÷2
÷32
÷64
÷12
TIMER 1
OVERFLOW
TIMER 2
OVERFLOW
SYSCLK

FIG. 32A

FIG. 32B


PORT I/O
TX
CROSSBAR
RX
CROSSBAR
SFR BUS
READ SBUF
822
SBUF
SERIAL PORT INTERRUPT
T1
R1
822
SBUF
ZERO DETECTOR
LOAD SBUF
SHIFT
INPUT SHIFT REGISTER (9 BITS)
SET
CLR
D
Q
SHIFT
DATA
SEND
Tx IRQ
Rx IRQ
LOAD SBUF
SHIFT
0x1FF
STOP BIT GENERATOR
START
Tx CONTROL
Tx CLOCK
ENABLE
MSB
Rx CONTROL
Rx CLOCK
START
TB8
REN
RB8
BIT DETECTOR
WRITE TO SBUF
SFR BUS
FROM FIG. 32A

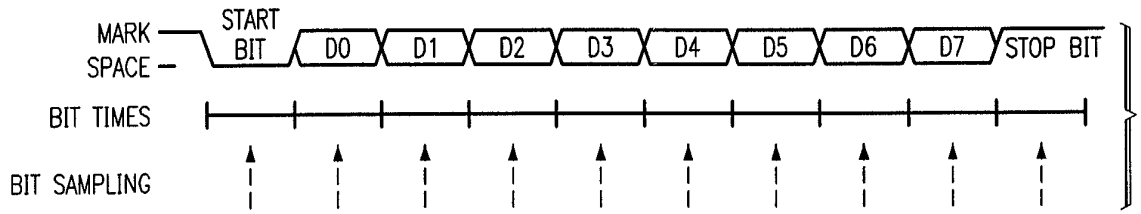


FIG. 35

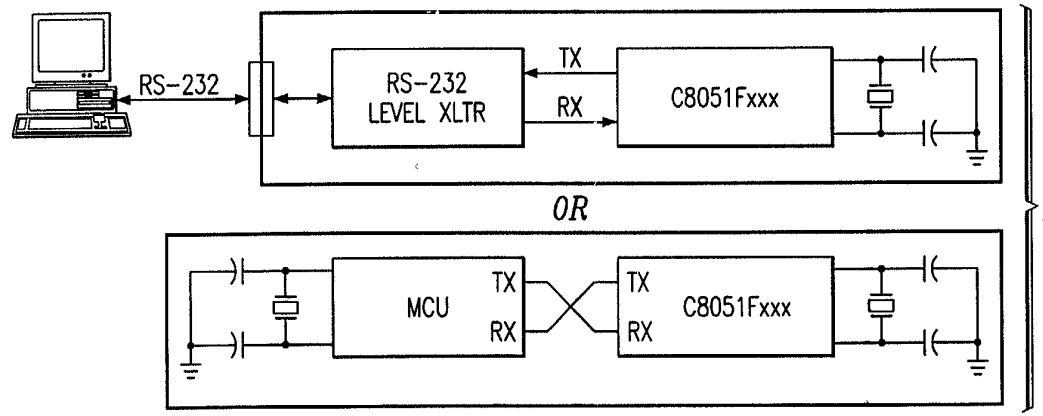


FIG. 36

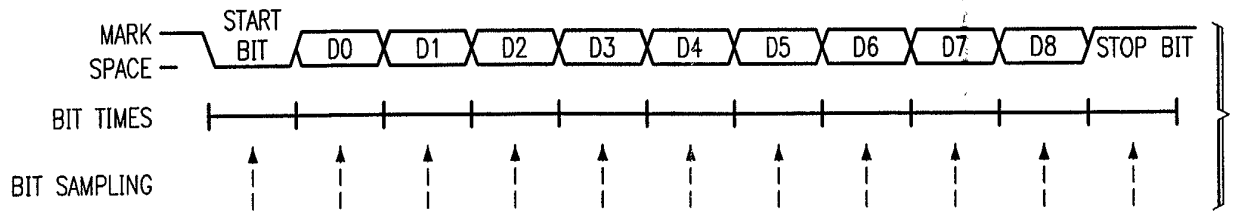


FIG. 37

FIG. 38

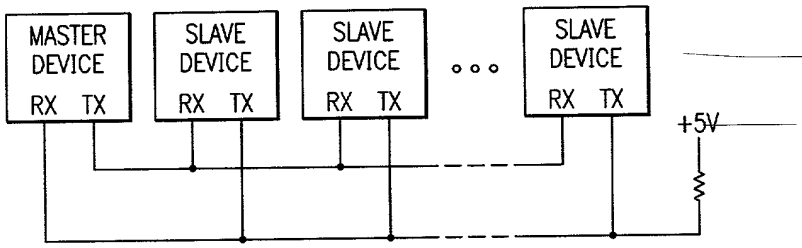
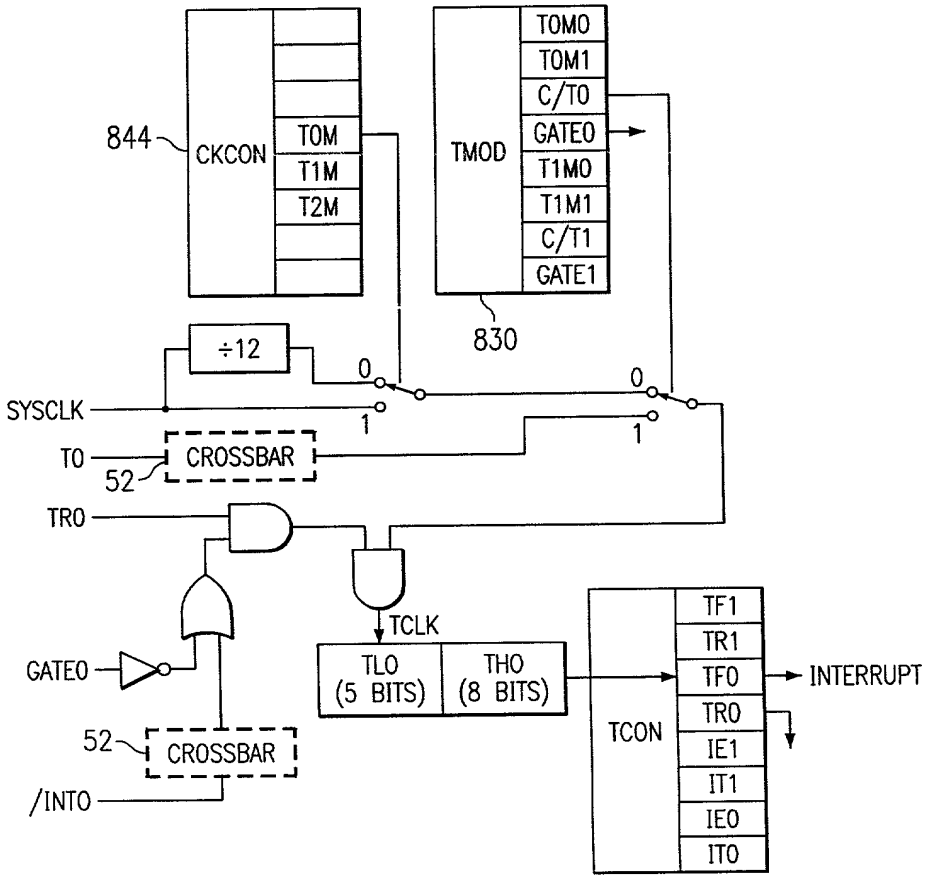

MASTER DEVICE
RX TX
SLAVE DEVICE
RX TX
SLAVE DEVICE
RX TX
SLAVE DEVICE
RX TX
+5V

FIG. 39


844
CKCON
T0M
T1M
T2M
TMOD
T0M0
T0M1
C/T0
GATE0
T1M0
T1M1
C/T1
GATE1
830
÷12
SYSCLK
T0
52
CROSSBAR
TR0
GATE0
52
CROSSBAR
/INT0
TCLK
TL0 (5 BITS)
TH0 (8 BITS)
TCON
TF1
TR1
TF0
TR0
IE1
IT1
IE0
IT0
INTERRUPT

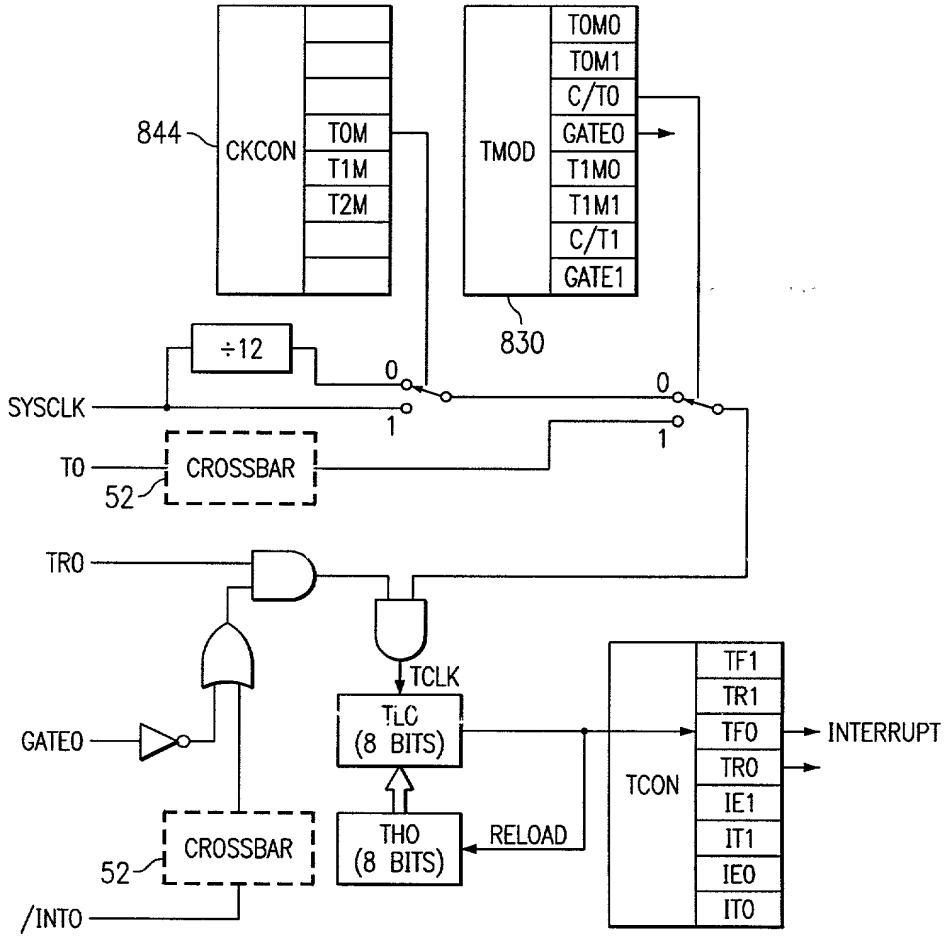

844
CKCON
T0M
T1M
T2M
TMOD
T0M0
T0M1
C/T0
GATE0
T1M0
T1M1
C/T1
GATE1
830
÷12
SYSCLK
0
1
0
1
T0
CROSSBAR
52
TR0
TCLK
GATE0
TLC
(8 BITS)
TCON
TF1
TR1
TF0
TR0
IE1
IT1
IE0
IT0
INTERRUPT
CROSSBAR
52
TH0
(8 BITS)
RELOAD
/INT0

FIG. 40

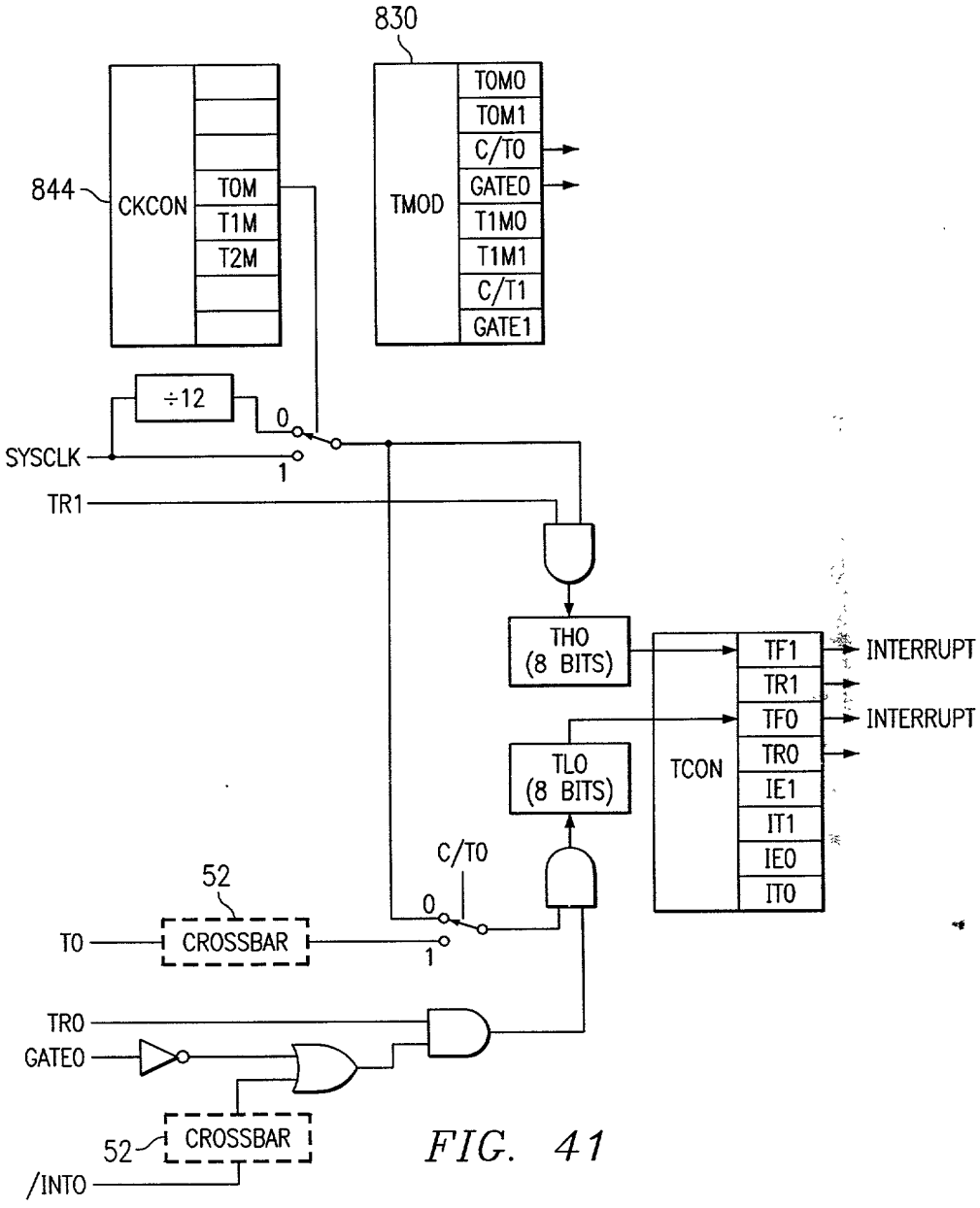

830
T0M0
T0M1
C/T0
GATE0
T1M0
T1M1
C/T1
GATE1
TMOD
844
CKCON
T0M
T1M
T2M
÷12
0
1
SYSCLK
TR1
TH0
(8 BITS)
TL0
(8 BITS)
TF1
TR1
TF0
TR0
IE1
IT1
IE0
IT0
TCON
INTERRUPT
INTERRUPT
C/T0
52
T0
CROSSBAR
TR0
GATE0
52
CROSSBAR
/INT0

FIG. 41

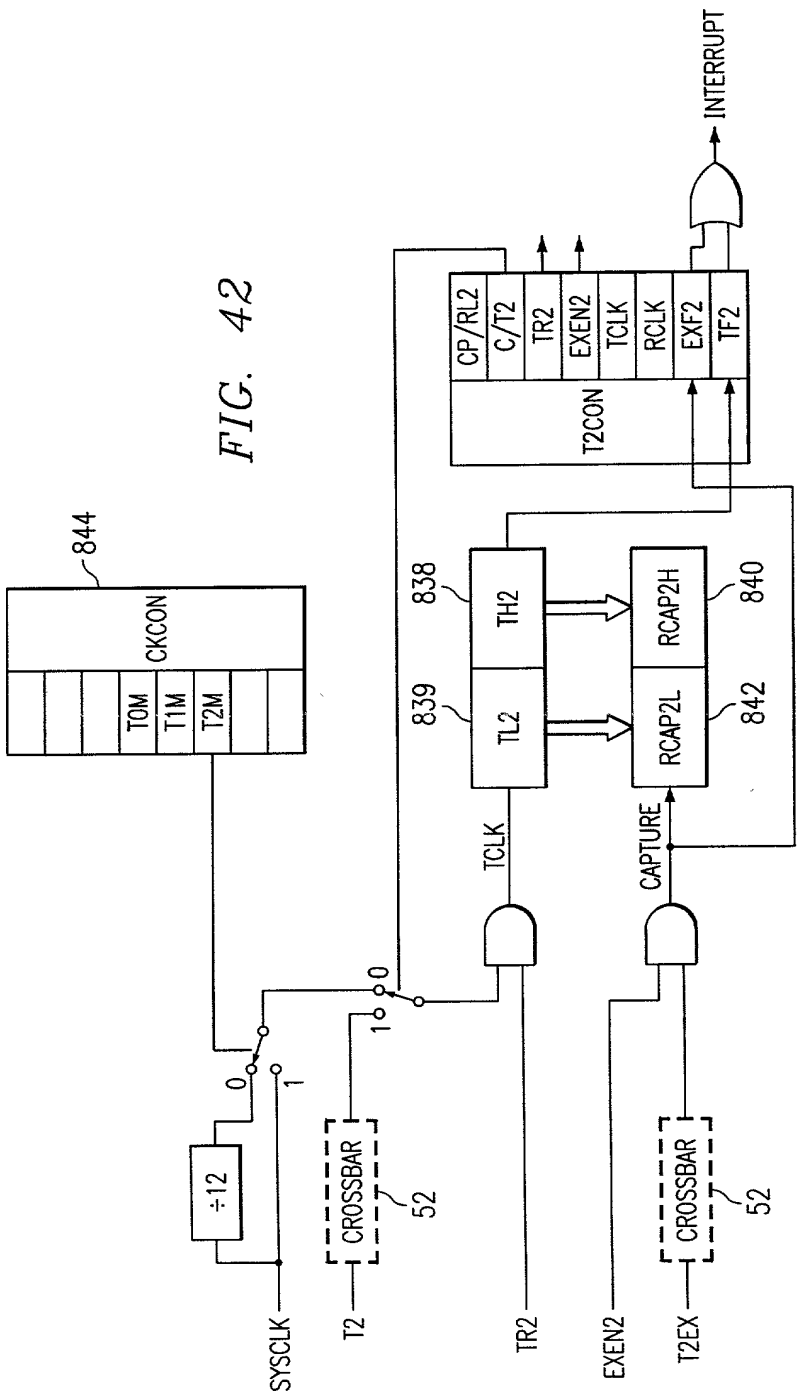
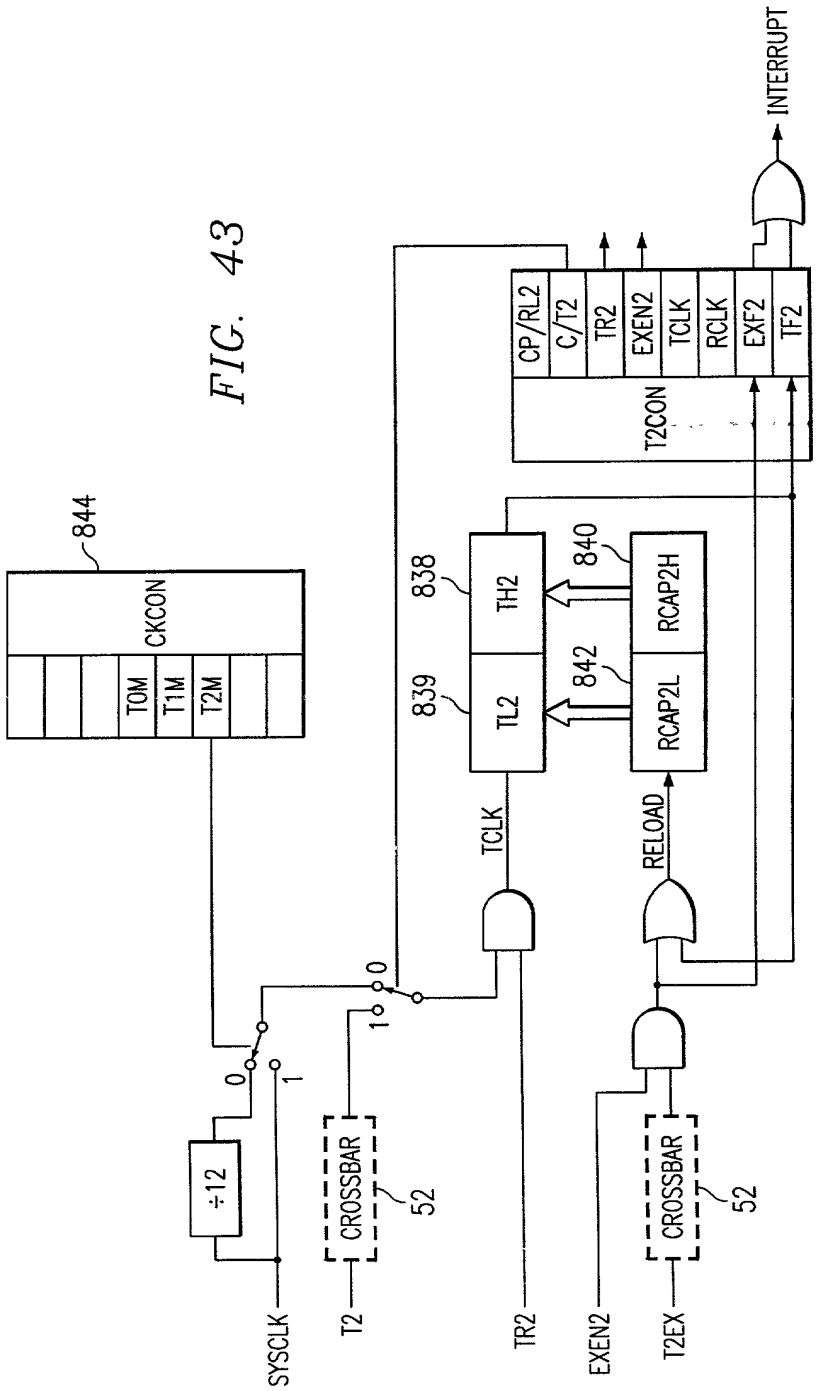

INTERRUPT
CP/RL2
C/T2
TR2
EXEN2
TCLK
RCLK
EXF2
TF2
T2CON
844
CKCON
T0M
T1M
T2M
838
TH2
RCAP2H
840
839
TL2
RCAP2L
842
TCLK
CAPTURE
0
1
0
1
÷12
CROSSBAR
52
CROSSBAR
52
SYSCLK
T2
TR2
EXEN2
T2EX

FIG. 42

FIG. 43


INTERRUPT
T2CON
CP/RL2
C/T2
TR2
EXEN2
TCLK
RCLK
EXF2
TF2
844
CKCON
T0M
T1M
T2M
838
TH2
840
RCAP2H
839
TL2
842
RCAP2L
TCLK
RELOAD
0
1
0
1
÷12
SYSCLK
CROSSBAR
52
T2
TR2
EXEN2
CROSSBAR
52
T2EX

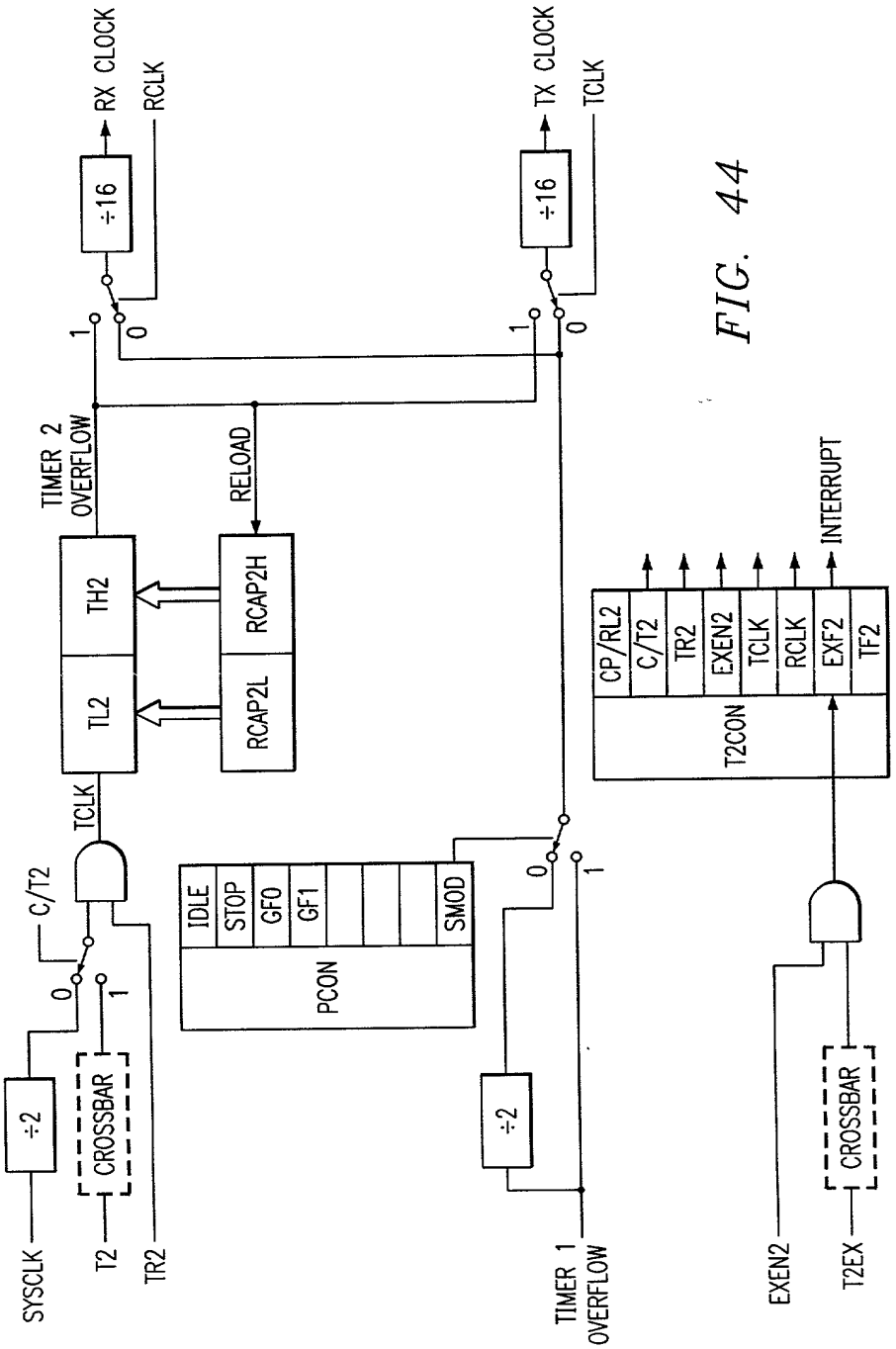

RX CLOCK
RCLK
÷16
TX CLOCK
TCLK
÷16
1
0
1
0
TIMER 2
OVERFLOW
RELOAD
TH2
TL2
RCAP2H
RCAP2L
TCLK
C/T2
0
1
IDLE
STOP
GF0
GF1
SMOD
PCON
0
1
CP/RL2
C/T2
TR2
EXEN2
TCLK
RCLK
EXF2
TF2
T2CON
INTERRUPT
÷2
CROSSBAR
÷2
SYSCLK
T2
TR2
TIMER 1
OVERFLOW
EXEN2
T2EX
CROSSBAR

FIG. 44

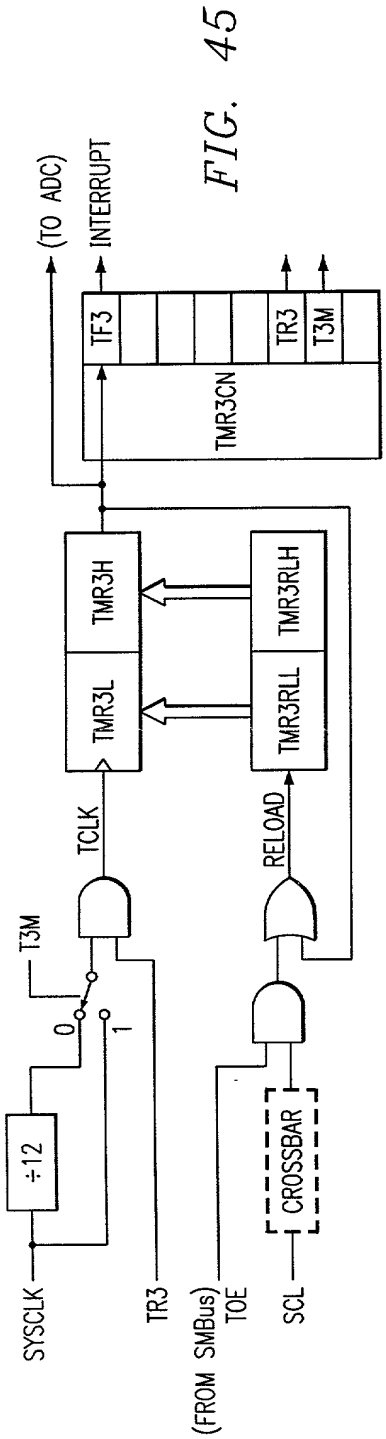

(TO ADC)
INTERRUPT
TF3
TMR3CN
TR3
T3M
TMR3H
TMR3L
TMR3RLH
TMR3RLL
TCLK
RELOAD
T3M
÷12
SYSCLK
TR3
(FROM SMBus)
TOE
SCL
CROSSBAR

FIG. 45

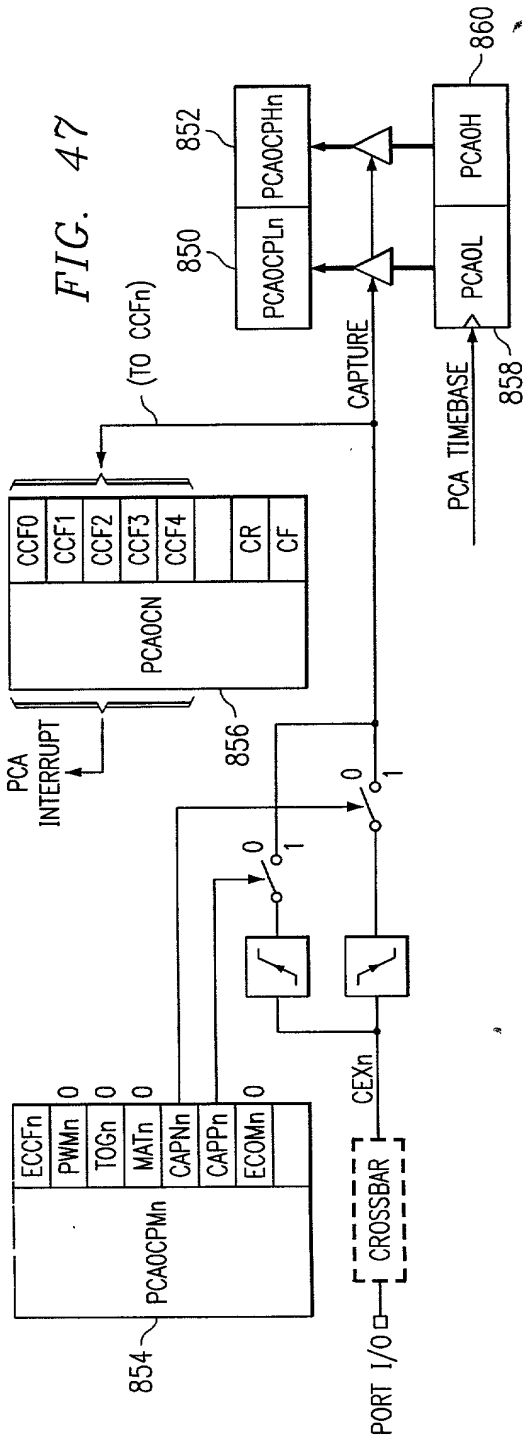
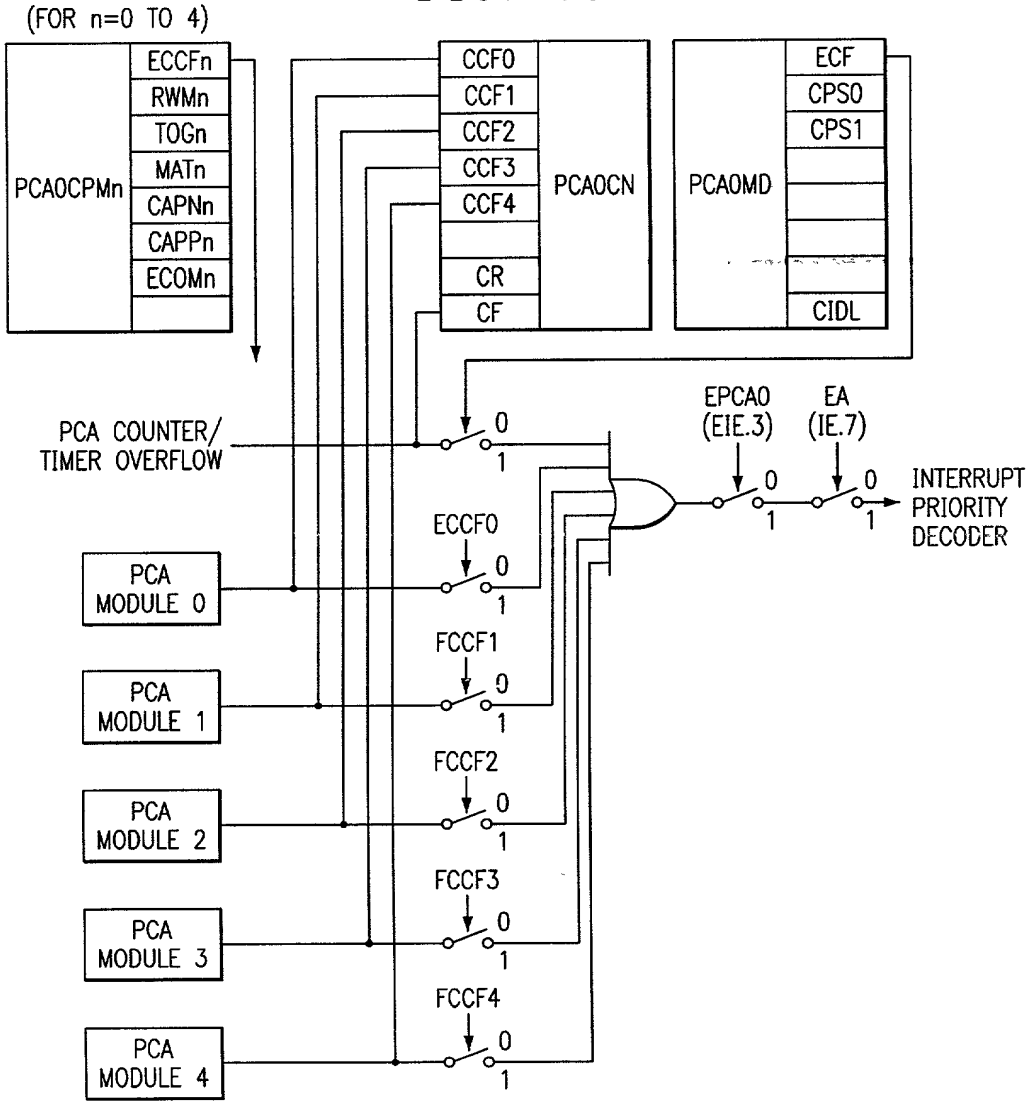

(TO CCFn)
CCF0
CCF1
CCF2
CCF3
CCF4
CR
CF
PCA0CN
PCA INTERRUPT
856
CAPTURE
852
PCA0CPHn
850
PCA0CPLn
860
PCA0H
PCA0L
PCA TIMEBASE
858
ECCFn
PWMn
TOGn
MATn
CAPNn
CAPPn
ECOMn
PCA0CPMn
854
CEXn
CROSSBAR
PORT I/O

FIG. 47

FIG. 46


(FOR n=0 TO 4)
PCA0CPMn
ECCFn
RWMn
TOGn
MATn
CAPNn
CAPPn
ECOMn
PCA0CN
CCF0
CCF1
CCF2
CCF3
CCF4
CR
CF
PCA0MD
ECF
CPS0
CPS1
CIDL
PCA COUNTER/
TIMER OVERFLOW
EPCA0
(EIE.3)
EA
(IE.7)
INTERRUPT
PRIORITY
DECODER
ECCF0
FCCF1
FCCF2
FCCF3
FCCF4
PCA
MODULE 0
PCA
MODULE 1
PCA
MODULE 2
PCA
MODULE 3
PCA
MODULE 4
0
1

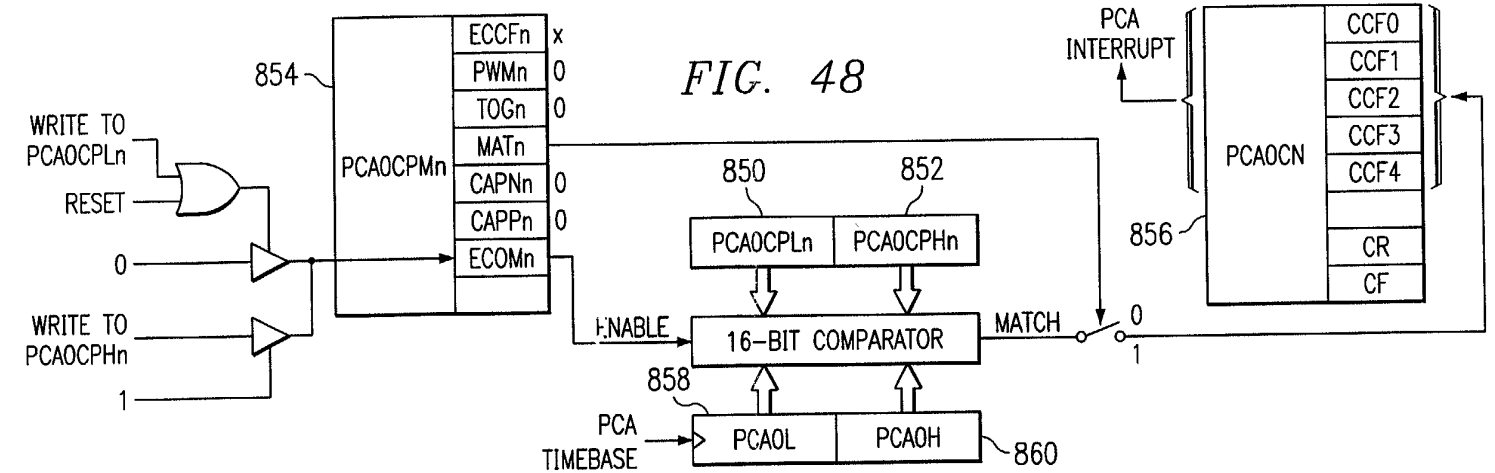

854
PCA0CPMn
ECCFn
PWMn
TOGn
MATn
CAPNn
CAPPn
ECOMn
x
0
0
0
0
0
WRITE TO PCA0CPLn
RESET
0
WRITE TO PCA0CPHn
1
850
852
PCA0CPLn
PCA0CPHn
ENABLE
16-BIT COMPARATOR
MATCH
858
PCA TIMEBASE
PCA0L
PCA0H
860
PCA INTERRUPT
PCA0CN
CCF0
CCF1
CCF2
CCF3
CCF4
CR
CF
856

FIG. 48

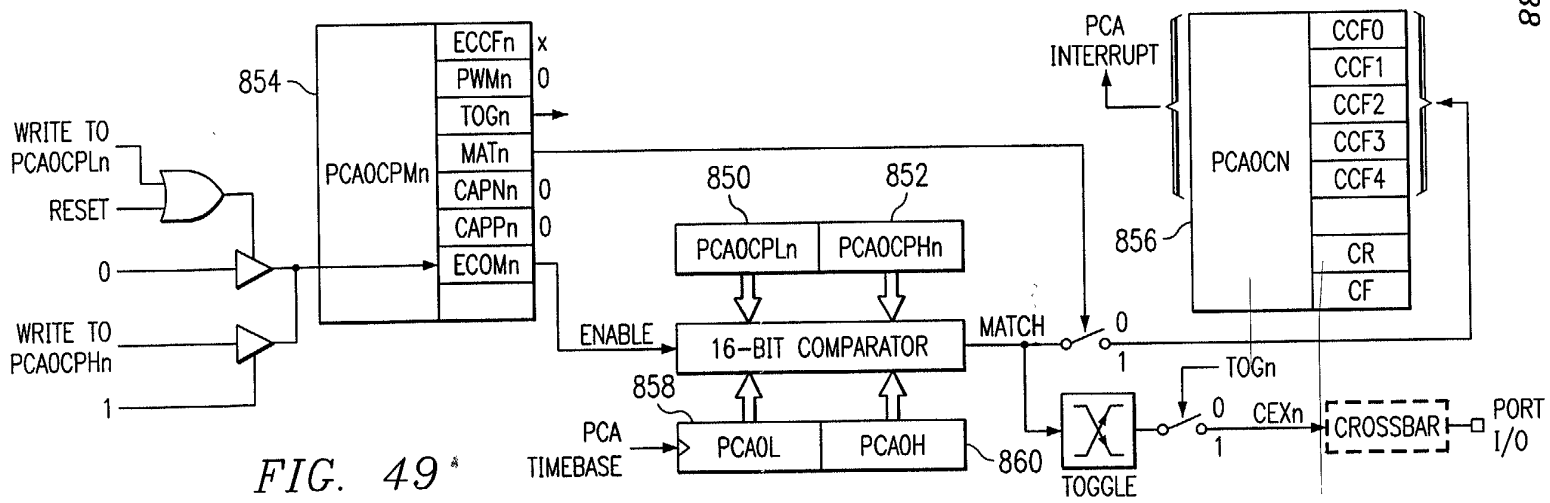

854
PCA0CPMn
ECCFn
PWMn
TOGn
MATn
CAPNn
CAPPn
ECOMn
x
0
0
0
0
WRITE TO PCA0CPLn
RESET
0
WRITE TO PCA0CPHn
1
850
852
PCA0CPLn
PCA0CPHn
ENABLE
16-BIT COMPARATOR
MATCH
858
PCA TIMEBASE
PCA0L
PCA0H
860
PCA INTERRUPT
PCA0CN
CCF0
CCF1
CCF2
CCF3
CCF4
CR
CF
856
TOGn
CEXn
CROSSBAR
PORT I/O
TOGGLE

FIG. 49

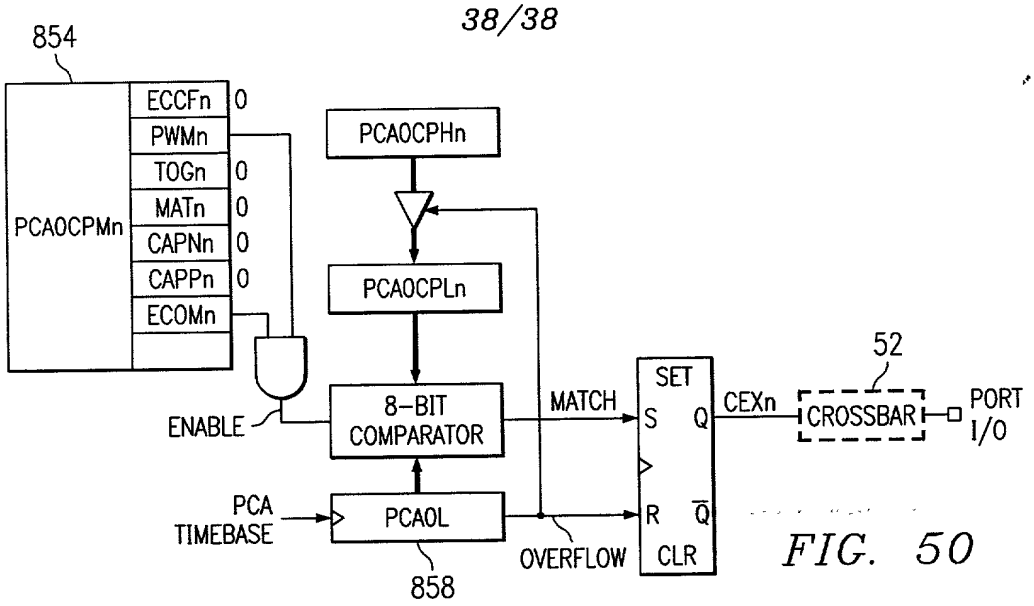

854
PCA0CPMn
ECCFn
PWMn
TOGn
MATn
CAPNn
CAPPn
ECOMn
0
0
0
0
0
PCA0CPHn
PCA0CPLn
ENABLE
8-BIT COMPARATOR
MATCH
SET
S
Q
R
Q
CLR
CEXn
52
CROSSBAR
PORT I/O
PCA TIMEBASE
PCA0L
858
OVERFLOW

FIG. 50

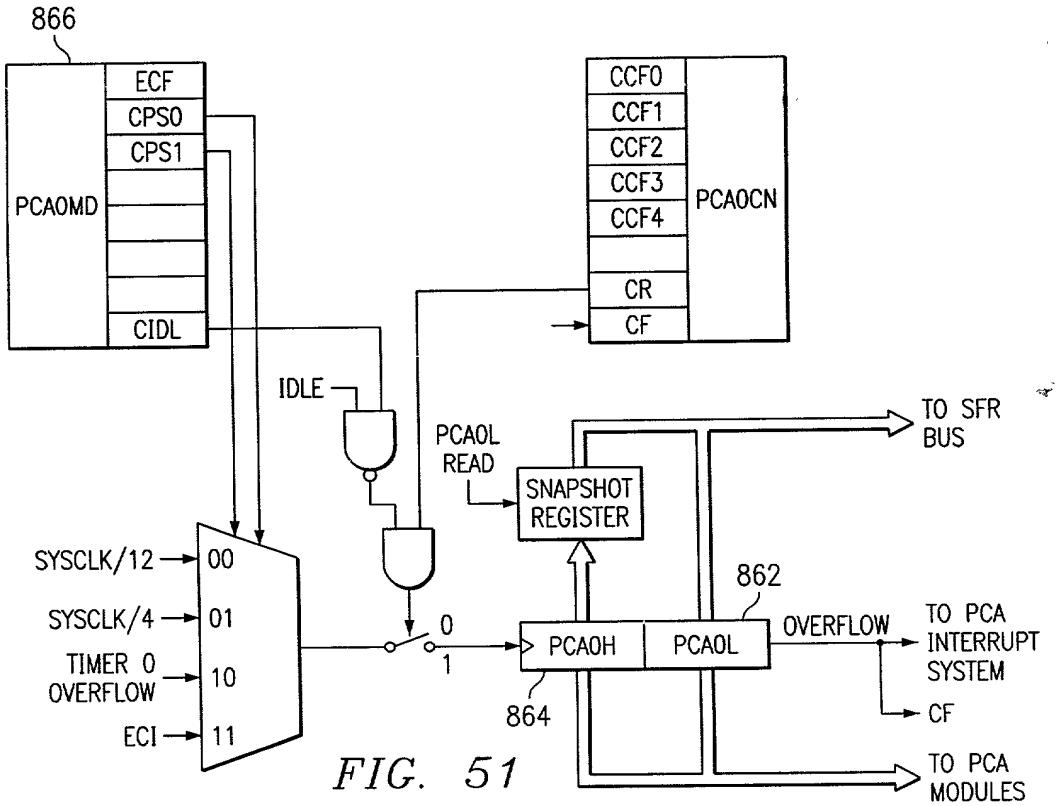

866
PCA0MD
ECF
CPS0
CPS1
CIDL
PCA0CN
CCF0
CCF1
CCF2
CCF3
CCF4
CR
CF
IDLE
PCA0L READ
SNAPSHOT REGISTER
TO SFR BUS
SYSCLK/12
SYSCLK/4
TIMER 0 OVERFLOW
ECI
00
01
10
11
0
1
862
PCA0H
PCA0L
OVERFLOW
TO PCA INTERRUPT SYSTEM
CF
TO PCA MODULES
864

FIG. 51